इंटरनेट मानक

Disclosure to Promote the Right To Information

Whereas the Parliament of India has set out to provide a practical regime of right to information for citizens to secure access to information under the control of public authorities, in order to promote transparency and accountability in the working of every public authority, and whereas the attached publication of the Bureau of Indian Standards is of particular interest to the public, particularly disadvantaged communities and those engaged in the pursuit of education and knowledge, the attached public safety standard is made available to promote the timely dissemination of this information in an accurate manner to the public.

"जानने का अधिकार, जीने का अधिकार"
Mazdoor Kisan Shakti Sangathan
"The Right to Information, The Right to Live"

"पुराने को छोड नये के तरफ"
Jawaharlal Nehru
"Step Out From the Old to the New"

IS 13516 (1993): Methods of Synthetic Testing of High Voltage Alternating Current Circuit-breakers [ETD 8: High Voltage Switchgear and Controlgear]

"ज्ञान से एक नये भारत का निर्माण"
Satyanarayan Gangaram Pitroda
"Invent a New India Using Knowledge"

Act Number 22 of 2005
The Indian Parliament
RIGHT TO INFORMATION

Made Available By
Public.Resource.Org

"ज्ञान एक ऐसा खजाना है जो कभी चुराया नहीं जा सकता है"
Bhartṛhari—Nītiśatakam
"Knowledge is such a treasure which cannot be stolen"

BLANK PAGE

BRUTUM FULMEN

IGNORANTIA
JURIS
NON EXCUSAT

PROTECTED BY COPYRIGHT

IS 13516 : 1993
IEC Pub 427 (1989)
(Reaffirmed 2003)

भारतीय मानक

उच्च वोल्टता प्रत्यावर्त्ती धारा परिपथ के संश्लिष्ट परीक्षण की पद्धतियाँ–वियोजक

Indian Standard

METHODS OF SYNTHETIC TESTING OF HIGH VOLTAGE ALTERNATING CURRENT CIRCUIT-BREAKERS

UDC 621·316·57·027·3 : 620·1

© BIS 1993

BUREAU OF INDIAN STANDARDS
MANAK BHAVAN, 9 BAHADUR SHAH ZAFAR MARG
NEW DELHI 110002

June 1993

Price Group 15

High Voltage Switchgear and Controlgear Sectional Committee, ETD 08

CONTENTS

Page

Clause

1. Introduction 1
2. Scope 1
3. Definitions 1

SECTION ONE — SYNTHETIC TESTING TECHNIQUES AND METHODS

4. Short-circuit breaking tests 2
   - 4.1 Basic principles and general requirements for synthetic breaking test methods 2
     - 4.1.1 High-current interval 3
     - 4.1.2 Interaction interval 4
     - 4.1.3 High-voltage interval 4
   - 4.2 Synthetic test circuits and related specific requirements for breaking tests 5
     - 4.2.1 Current injection methods 5
     - 4.2.2 Voltage injection method 6
     - 4.2.3 Duplicate circuit method (transformer or Skeats circuit) ... 7
     - 4.2.4 Other synthetic test methods 7
5. Short-circuit making tests 7
   - 5.1 Basic principles and general requirements for synthetic making test methods 7
     - 5.1.1 High-voltage interval 8
     - 5.1.2 Pre-arcing interval 8
     - 5.1.3 Latching interval and fully closed position ... 9
   - 5.2 Synthetic test circuit and related specific requirements for making tests 9
     - 5.2.1 Test circuit 9
     - 5.2.2 Specific requirements 9
   - 5.3 Evaluation of the maximum pre-arcing time 9

SECTION TWO — SPECIFIC REQUIREMENTS FOR SYNTHETIC TESTS FOR MAKING AND BREAKING PERFORMANCE RELATED TO THE REQUIREMENTS OF SUB-CLAUSES 6.102 TO 6.111 INCLUSIVE OF IEC PUBLICATION 56

6.102.1.3 Multi-part testing 10
6.102.2 Arrangement of circuit-breaker for tests... ... 10
6.102.9 Circuit-breakers with short arcing times... ... 10
6.106 Basic short-circuit test-duties ... 10
6.106.1-2-3 Test-duties Nos. 1, 2 and 3 11
6.106.4 Test-duty No. 4 11
6.106.5 Test-duty No. 5 12
6.109 Short-line fault tests 13
6.111 Synthetic methods for capacitive-current switching ... 13
TABLES I TO V 14
FIGURES 1 TO 6 19
APPENDIX AA Current distortion 25

(Continued on third cover)

Indian Standard

METHODS OF SYNTHETIC TESTING OF HIGH VOLTAGE ALTERNATING CURRENT CIRCUIT-BREAKERS

1. Introduction

During the past few decades experience has been gained with synthetic testing techniques and methods. It has been proven that synthetic testing is an economical and technically correct way to test high-voltage a.c. circuit-breakers according to the requirements of IEC Publication 56.

This is why it was decided to include synthetic testing methods, after a thorough revision of the first edition of IEC Publication 427, as equivalent to the direct test methods.

2. Scope

This standard applies to a.c. circuit-breakers within the scope of IEC Publication 56 (Clause 1). It provides the general rules for testing a.c. circuit-breakers, for making and breaking capacities over the range of test-duties described in Sub-clauses 6.102 to 6.111 of IEC Publication 56, by synthetic methods.

Note. — Circuits for the test duties described in Sub-clause 6.111 have not yet been standardized. However, present methods are given in Appendix GG.

The methods and techniques described are those in general use. The purpose of this standard is to establish criteria for synthetic testing and for the proper evaluation of results. Such criteria will establish the validity of the test method without imposing restraints on innovation of test circuitry.

3. Definitions

The definitions of IEC Publication 56 and the following definitions apply:

3.1 *Direct test*

A test in which the applied voltage, the current and the transient and power-frequency recovery voltages are all obtained from a circuit having a single-power source, which may be a power system or special alternators as used in short-circuit testing stations or a combination of both.

3.2 *Synthetic test*

A test in which all of the current, or a major portion of it, is obtained from one source (current circuit), and in which the applied voltage and/or the recovery voltages (transient and power-frequency) are obtained wholly or in part from one or more separate sources (voltage circuits).

3.3 *Test circuit-breaker*

The circuit-breaker under test (see Sub-clause 6.102.2 of IEC Publication 56).

3.4 *Auxiliary circuit-breaker(s)*

The circuit-breaker(s) forming part of a synthetic test circuit used to put the test circuit-breaker into the required relation with various circuits.

3.5 *Current circuit*

That part of the synthetic test circuit from which all or the major part of the power-frequency current is obtained.

3.6 *Voltage circuit*

That part of the synthetic test circuit from which all or the major part of the test voltage is obtained.

3.7 *Prospective current* (of a circuit and with respect to a circuit-breaker) (IEV 441-17-01 modified)

The current that would flow in the circuit if each pole of the test and auxiliary circuit-breakers were replaced by a conductor of negligible impedance.

3.8 *Actual current*

The current through the test circuit-breaker (prospective current modified by the arc-voltage of the test and auxiliary circuit-breakers).

3.9 *Distortion current*

A calculated current equal to the difference between the prospective current and the actual current.

3.10 *Post-arc current*

The current which flows through the arc-gap of a circuit-breaker immediately after the current and arc-voltage have fallen to zero and the transient recovery voltage has begun to rise.

3.11 *Current-injection method*

A synthetic test method in which the voltage circuit is applied to the test circuit-breaker before power-frequency current-zero.

3.12 *Injected current*

The current supplied by the voltage circuit of a current injection circuit when it is connected to the circuit-breaker under test.

3.13 *Voltage-injection method*

A synthetic test method in which the voltage circuit is applied to the test circuit-breaker after power-frequency current-zero.

3.14 *Reference system conditions*

The conditions of an electrical system having the parameters from which the rated and test values of IEC Publication 56 are derived.

SECTION ONE — SYNTHETIC TESTING TECHNIQUES AND METHODS

4. **Short-circuit breaking tests**

4.1 *Basic principles and general requirements for synthetic breaking test methods*

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally, the adequacy is established when the test method meets the requirements set forth in the following sub-clauses.

Basic intervals

A circuit-breaker has two basic positions: closed and open. In the closed position a circuit-breaker conducts full current with negligible voltage drop across its contacts. In the open position it conducts negligible current but with full voltage across the contacts. This defines the two main stresses, the current stress and the voltage stress, which are separated in time.

If closer attention is paid to the voltage and current stresses during the interrupting process (Figure 1), three main intervals can be recognized:

- High-current interval

  The high-current interval is the time from contact separation to the start of the significant change in arc-voltage. The high-current interval precedes the interaction and high-voltage intervals.

- Interaction interval

  The interaction interval is the time from the start of the significant change in arc-voltage prior to current-zero to the time when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker. (See also Appendix BB2).

- High-voltage interval

  The high-voltage interval is the time from the moment when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker to the end of the test.

4.1.1 *High-current interval*

During this interval the test circuit-breaker shall be stressed by the test circuit in such a way that the starting conditions for the interaction interval, within tolerances to be specified, are the same as under reference system conditions.

In synthetic test circuits the ratio of the power-frequency voltage of the current circuit to the arc-voltage is low in comparison with tests at reference system conditions due to:

- the voltage of the current circuit being a fraction of the system voltage;
- the fact that the arc-voltages of the test circuit-breaker and of the auxiliary circuit-breaker are added.

As a result the duration of the current loop and the peak value of the current will be reduced. This distortion of the current is outlined in Appendix AA.

Considerations with respect to the arc-energy released in the test circuit-breaker lead to a maximum permissible influence in terms of tolerances on two characteristic values of the shape of the current, i.e. current-peak value and current-loop duration (see Appendix AA).

The tolerance on the amplitude and the power frequency of the prospective breaking current, as given in Sub-clauses 6.103.2 and 6.104.3 of IEC Publication 56, shall not be exceeded by the actual current through the test circuit-breaker. Therefore the following conditions shall be met:

- the actual current amplitude during the last loop in the test circuit-breaker shall comply with the requirements for the prospective current stated in Sub-clause 6.104.3 of IEC Publication 56. The amplitude of the final loop of the actual test current in a single phase circuit shall be not less than 90% of the value specified;
- the duration of the final loop of the actual power-frequency test current shall be not less than 90% of the loop duration given by the rated frequency after taking into account, where this is appropriate, the effect of the specified d.c. component;
- when performing synthetic tests on circuit-breakers possessing arc-voltage characteristics which would significantly modify the current in service, the influence of the arc-voltage on the current

amplitude and loop duration may be allowed for when considering the tolerances given above.

The detailed procedure for estimating these corrections with examples for establishing the tolerances is given in Appendix AA.

To keep within the tolerances for the test current, it is acceptable to increase the current by increasing the voltage or reducing the reactance of the current circuit, or to apply a current with an increased d.c. component or a reduced power frequency. For this purpose the specified tolerances for d.c. component and power frequency may be exceeded subject to the consent of the manufacturer.

4.1.2 *Interaction interval*

During the interaction interval, the short-circuit current stress changes into high-voltage stress and the circuit-breaker performance can significantly influence the current and voltages in the circuit. As the current decreases to zero, the arc voltage may rise to charge parallel capacitance and distort current passing through the arc. After the current-zero the post-arc conductivity may result in additional damping of the transient recovery voltage and thus influence the voltage across the circuit-breaker and the energy supplied to the ionised contact gap. The interaction between the circuit and the circuit-breaker immediately before and after current-zero (i.e. during the interaction interval) is of extreme importance to the interrupting process.

During the interaction interval the current and voltage wave forms shall be the same for a synthetic test as under reference system conditions (Sub-clause 3.14), taking into account the possible deviations of the current and voltage from the prospective values due to the interaction between the circuit-breaker and the circuit.

The interaction interval presents the critical time for the thermal failure mode of the circuit-breaker. Therefore, it is of extreme importance that the shape and magnitude of the prospective transient recovery voltage (TRV) corresponds to that associated with the prospective current of the relevant test-duty.

The above implies strict requirements for the test circuit. The requirements are given for the current injection method in Sub-clause 4.2.1 and for the voltage injection method in Sub-clause 4.2.2.

Note. — Depending on the test circuit used, the interaction between circuit and test circuit-breaker may be disturbed by the behaviour of the auxiliary circuit-breaker during the critical interval around current-zero.
The arc-voltage of the auxiliary circuit-breaker should be less than or equal to the arc-voltage of the test circuit-breaker.
If an auxiliary circuit-breaker with a higher arc-voltage is used, a higher power-frequency voltage of the current circuit may be necessary.

4.1.3 *High-voltage interval*

During the high-voltage interval the gap of the test circuit-breaker is stressed by the recovery voltage.

The prospective TRV shall comply with the requirements of Sub-clauses 4.102, 4.105, 4.106 and 6.104.5 of IEC Publication 56. Suitable methods for determining the prospective TRV in synthetic test circuits can be selected from Appendix GG of IEC Publication 56.

The impedance of the voltage circuit shall be low enough to give clear evidence of breakdown, if any.

Notes 1. — If the test circuit-breaker is fitted with low ohmic parallel resistors, a special procedure may be necessary (see Appendix FF).

2. — If the TRV is obtained from more than one source the overall wave shape should not show any appreciable discontinuity.

In principle, the power-frequency recovery voltage for the basic short-circuit test-duties shall equate with the requirements of Sub-clause 6.104.7 of IEC Publication 56. In synthetic testing the recovery voltage is supplied from the voltage circuit, either directly or in series with the current circuit. This gives a d.c. voltage, or a combined a.c. and d.c. voltage, or an a.c. voltage, which in most cases decays due to the limited energy of the voltage source. It may thus not be possible to maintain the recovery voltage for at least 0,1 s as specified in Sub-clause 6.104.7 of IEC Publication 56. Deviations from the specified recovery voltage are acceptable if the following conditions are met:

- The instantaneous value of the recovery voltage during a period equal to 1/8 of a cycle of the rated frequency of the circuit-breaker shall be not less than the equivalent instantaneous value of the power-frequency recovery voltage specified in Sub-clause 6.104.7 of IEC Publication 56 which starts with a minimum peak value of 0,95 $h\sqrt{2}\ U/\sqrt{3}$.

  h = first pole-to-clear factor (1,3 or 1,5).
  U = rated voltage of the circuit-breaker.

- Whether an exponentially decaying d.c., an a.c. or a combined a.c. and d.c. recovery voltage is used, its instantaneous value (for d.c.) or its peak value (or a.c. or combined a.c. and d.c) should in principle be kept as close as possible to $\sqrt{2}\ U/\sqrt{3}$ and in any case must not fall below 0,5 $\sqrt{2}\ U/\sqrt{3}$ in less than 0,1 s (see Figure 2).

- If an exponentially decaying d.c. or a combined a.c. and d.c. recovery voltage imposes an inappropriate stress on the circuit-breaker compared to that due to the specified a.c. recovery voltage in reference system conditions, then a more appropriate circuit may be used taking into account Sub-clause 6.104.7 of IEC Publication 56 and also the limits stated above.

4.2 *Synthetic test circuits and related specific requirements for breaking tests*

4.2.1 *Current injection methods*

These methods can be described in terms of general principles as follows (see Appendix BB):

- the current from the voltage source is superimposed on the current in the test circuit-breaker prior to the interaction interval;
- an auxiliary circuit-breaker interrupts the current from the current circuit prior to the interaction interval.

During the interaction interval the test circuit-breaker is exposed to the voltage of the voltage circuit having an impedance which is representative of the reference system conditions. This explains the validity of current injection methods. Several current injection methods are known but only the conditions for parallel current injection are given below since this method is used by the majority of the test laboratories. The following conditions shall be met:

a) TRV wave-shaping circuit

1) The shape and magnitude of the prospective TRV shall comply with the specified values.
2) Ideally the equivalent surge impedance Z_h (see Figure 3) shall be equal to $(du/dt)/(di/dt)$ during the interaction interval. du/dt is the rate of rise of the specified transient recovery voltage and di/dt is the rate of decrease of the specified short-circuit current.
3) The combination of the stray and lumped capacitance C_{dh} in parallel with Z_h gives rise to the delay time $t_d = Z_h C_{dh}$.

b) Inductance of the voltage circuit

The value of the inductance of the voltage circuit shall be between 1,0 and 1,5 times the inductance derived from the equivalent power-frequency voltage divided by the prospective current.

c) Frequency of the injected current and the injection timing

The frequency of the injected current shall preferably be of the order of 500 Hz with a lower limit of 250 Hz and an upper limit of 1 000 Hz.

The initiation of the injected current shall be adjusted such that the time, during which the test circuit-breaker is fed only by the injected current, is not more than a quarter of the period of the injected current frequency with a maximum of 500 µs.

In order to prevent undue influence on the wave shape of the power-frequency current, the lower limit of the frequency of the injected current is 250 Hz.

The maximum frequency of the injected current is determined by the interval of significant change of arc-voltage, which interval shall be smaller than the time for which the arc is fed only by the injected current. To achieve this, the period of the injected frequency should be at least four times the interval of significant change of arc-voltage (see Appendix BB).

Note. — Attention should be paid to the possible overstressing of the circuit-breaker if the time that the test circuit-breaker is fed by the injected current only is less than 200 µs.

d) Waveshape of the injected current

The prospective rate of decrease (d*i*/d*t*) of the injected current shall correspond to that of the prospective power-frequency current.

The injected current shall be practically free of superimposed oscillations for a time not less than 100 µs before current-zero.

4.2.2 *Voltage injection method*

Several voltage injection methods are known but only series voltage injection is described here in general terms as follows (see also Appendix CC):

- The voltage from the voltage circuit is applied to the test circuit-breaker after the interaction interval.
- An auxiliary circuit-breaker with a parallel capacitor is used to apply the recovery voltage to the test circuit-breaker.
- During the high-current and interaction intervals the test circuit-breaker is exposed to the current circuit only.

If the voltage injection method is to be used to check the thermal behaviour of the circuit-breaker, i.e. to test under terminal fault conditions with initial transient recovery voltage (ITRV) stress or under short-line-fault conditions, it is necessary to demonstrate the validity of the test circuit for the interaction interval. This is subject to agreement between manufacturer, testing station and user.

When used for tests relating to the dielectric behaviour of the circuit-breaker, the following conditions shall be met:

- the auxiliary circuit-breaker should have an arc-voltage less than or equal to that of the test circuit-breaker. This condition is met if the extinction peaks of both circuit-breakers are approximately the same (see note in Sub-clause 4.1.2);
- the impedance of the voltage circuit shall be low enough to provide for reignitions or restrikes if they occur.

Therefore, the capacitance across the auxiliary circuit-breaker shall be at least 10 nF. Care should be taken to avoid undue distortion of the current before power-frequency current-zero;

- no pause shall be introduced by the combining of the current circuit and the voltage circuit.

Note. — For short-line fault tests, in addition to the voltage injection circuit supplying the source side TRV, a current injection circuit which is connected to the line-side terminal of the test circuit-breaker can be used to supply the line-side transient voltage.

4.2.3 *Duplicate circuit method (transformer or Skeats circuit)*

This method can be described in terms of general principles as follows (see also Appendix DD):

- the current and voltage are supplied from the same source;
- the a.c. recovery voltage is supplied from a step-up transformer the primary of which is connected to the current circuit;
- the recovery voltage is applied to the test circuit-breaker through an impedance (normally a resistance).

The auxiliary circuit-breaker interrupts the current prior to the test circuit-breaker by a short time interval (usually about 10 µs). During this short interval the value of d*i*/d*t* of the current in the test circuit-breaker is decreased.

The test circuit is therefore not valid for tests where attention is paid to the thermal failure mode of the test circuit-breaker.

The test circuit is suitable for testing the dielectric behaviour of a circuit-breaker.

The test circuit can be used for making tests.

The test circuit can easily be adapted to supply full voltage stresses in two (or more) operations e.g. at both closing and opening in a CO operation, at both openings in an O$-t-$CO operation or even at consecutive current-zeros in an opening operation. See Appendix DD.

4.2.4 *Other synthetic test methods*

Other methods may prove correct and advantageous for testing of circuit-breakers with specific characteristics or for testing of a circuit-breaker for specific performance. Even though these methods are not covered by this standard, they can be used subject to understanding of their application and agreement between the manufacturer and the user.

Synthetic methods for three-phase short-circuit breaking tests and load-current switching tests are known. However, in some cases there are no requirements in IEC Publication 56 (e.g. TRV values for the last phases to clear in three-phase circuits). In other cases there still is a lack of experience. In order to reflect the present position and to have these methods available, they are described in the following appendices:

- Appendix FF – Special procedures for testing circuit-breakers having parallel breaking resistors;
- Appendix HH – Synthetic methods for three-phase testing.

5. **Short-circuit making tests**

5.1 *Basic principles and general requirements for synthetic making test methods*

During a closing operation onto a short-circuit, the circuit-breaker contact gap is subjected to the applied voltage corresponding to the r.m.s. value of the rated voltage divided by $\sqrt{3}$ which causes its breakdown. After this moment, the circuit-breaker is subjected to the making current which is expressed by its maximum amplitude $\hat{i}$ in Figure 4 (see Sub-clause 4.103 of IEC Publication 56).

In a synthetic test circuit the applied voltage is supplied by a separate voltage source and the short-circuit current is supplied by a reduced voltage current circuit. This latter is connected to the circuit-breaker immediately after breakdown of the contact gap by means of a fast making device, e.g. a triggered spark gap.

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally the adequacy is established when the test method meets the requirements set forth in the following sub-clauses.

Basic intervals

Prior to making, a circuit-breaker withstands the rated phase-to-earth voltage applied across its terminals: during making, it carries the rated short-circuit current. If closer attention is paid to the voltage and current stresses during the making test—Figure 4—three main intervals can be recognised:

- High-voltage interval

  The high-voltage interval is the time from the commencement of the test, with the circuit-breaker in the open position, to the moment of breakdown across the contact gap.

- Pre-arcing interval

  The pre-arcing interval is the time, during the closing stroke of the circuit-breaker, from the moment of breakdown across the contact gap to the touching of the contacts.

- Latching interval

  The latching interval is the time, during the closing stroke of the circuit-breaker, from the touching of the contacts to the moment when the contacts reach the fully closed (latched) position.

5.1.1 *High-voltage interval*

During this interval the circuit-breaker shall be stressed by the test circuit in such a way that the starting conditions for the pre-arcing interval, within the tolerances to be specified, are the same as under reference system conditions.

Therefore the following conditions shall be met:

- The applied voltage shall comply with the requirement set forth in Sub-clause 6.104.1 of IEC Publication 56.
- The phase relationship between the applied voltage and the short-circuit current shall correspond to the rated power factor of the test circuit within the tolerances given in Sub-clause 6.103.1 of IEC Publication 56.

However, when performing synthetic tests on circuit-breakers having a high closing speed and consequently a short pre-arcing time a reduced applied voltage can be used provided that the maximum pre-arcing time determined in accordance with Sub-clause 5.3 does not exceed $1/\omega$ s (3.2 ms for 50 Hz and 2.7 ms for 60 Hz) as shown in Figure 5.

5.1.2 *Pre-arcing interval*

During pre-arcing the circuit-breaker is subjected to electrodynamic forces due to the current and to deteriorating effects due to arc-energy. In general the current is composed of three components:

- the initial transient making current, ITMC,
- the d.c. and a.c. components of the short-circuit current.

Two typical cases may occur depending on the moment of closing and on the circuit-breaker design:

- Breakdown occurs near the crest of the applied voltage; an almost symmetrical current is established. Pre-arc energy and ITMC are relatively high.

- Breakdown occurs near zero of the applied voltage; an asymmetrical current is established. Pre-arc energy and ITMC are negligible with the exception of the case of non-simultaneous closing in a multi-unit pole.

Note. – The ITMC is not defined in Sub-clause 4.103 of IEC Publication 56; a value sufficient to maintain pre-arcing is adequate.

5.1.3 *Latching interval and fully closed position*

During these intervals the circuit-breaker has to close in presence of the electrodynamic forces due to the current and contact friction forces. Therefore during these intervals the making current shall comply with Sub-clause 4.103 of IEC Publication 56.

5.2 *Synthetic test circuit and related specific requirements for making tests*

5.2.1 *Test circuit*

The test circuit is made up with two sources namely the current and the voltage circuit as shown in Figure 6.

- The voltage circuit, which mainly consists of a low power transformer, supplies:
  - the applied voltage during the high-voltage interval;
  - the ITMC during the pre-arcing interval, by the discharge of the ITMC-circuit.
- The current circuit supplies the making current during the pre-arcing, and latching intervals.

5.2.2 *Specific requirements*

During a synthetic making test the phase relationship between the applied test voltage and the short-circuit current depends on the following parameters:

- phase displacement between the current source voltage u_1 and the voltage source voltage u_2;
- delay time of making gap;
- minimum sparkover voltage of making gap.

The phase displacement between the applied voltage and the short-circuit current shall be 90 ± 27 electrical degrees.

The injected current supplied by the voltage circuit ensures pre-arcing before the closing of the fast make gap. Therefore the time constant of ITMC-circuit shall be longer than the make gap delay time.

Note. – The voltage source u_2 may be an a.c. or a d.c. source.

5.3 *Evaluation of the maximum pre-arcing time*

To determine whether a reduced applied voltage can be used for the making test, the maximum pre-arcing time of the circuit-breaker has to be established. (See Sub-clause 5.1.1). This maximum pre-arcing time shall be determined by preliminary direct tests carried out at full voltage and at the maximum short-circuit current available. To ensure this, pre-arcing should commence at the peak of the voltage wave. The current should ensure decisive breakdown during the pre-strike.

During rated operating sequences making operations are preceded by breaking operations, e.g. O–t–CO–t'–CO or CO–t''–CO.

Therefore the following tests shall be carried out:

O $-t-$ CO $-t'-$ CO with:

t = 3 min for circuit-breakers not intended for rapid auto-reclosing

t = 0,3 s for circuit-breakers intended for rapid auto-reclosing

t' = 3 min.

or CO $-t''-$ CO with:

t'' = 15 s.

SECTION TWO – SPECIFIC REQUIREMENTS FOR SYNTHETIC TESTS FOR MAKING AND BREAKING PERFORMANCE RELATED TO THE REQUIREMENTS OF SUB-CLAUSES 6.102 TO 6.111 INCLUSIVE OF IEC PUBLICATION 56

Sub-clauses 6.102 to 6.111 inclusive of IEC Publication 56 are also applicable for synthetic testing. However, in some cases special techniques are necessary. These cases are mentioned in the sub-clauses of this section. The numbering of the sub-clauses corresponds to that of IEC Publication 56.

6.102.1.3 *Multi-part testing*

For synthetic methods for the testing of circuit-breakers fitted with low-ohmic parallel resistors see Appendix FF.

6.102.2 *Arrangement of circuit-breaker for tests*

For synthetic methods for three-phase circuits see Appendix HH.

6.102.9 *Circuit-breakers with short arcing times*

In order to be able to perform synthetic tests on the same basis as direct tests, normally it will be necessary to apply special reignition methods to prolong the arcing of the test circuit-breaker through the necessary number of zeros of the power-frequency current. It may be necessary to make some tests in order to obtain the actual range of arcing times of the test circuit-breaker. See Appendix JJ for reignition methods to prolong arcing.

Note. – Although this sub-clause refers to circuit-breakers with short arcing times, in principle the same arc-prolongation methods can be used for circuit-breakers with longer arcing times.

6.106 *Basic short-circuit test-duties*

The operating sequences for test-duties Nos. 1, 2, 3 and 5 together with the various methods of carrying out test-duty No. 4 are shown in Table I.

Symbols: C_S = Making operation with specified parameters in a synthetic circuit.

O_S = Breaking operation with specified parameters in a synthetic circuit.

C_D = Making operation with reduced applied voltage of the curent source only and the specified making current.

O_D = Breaking operation with reduced transient and power-frequency recovery voltages of the current source only and with the specified breaking current.

Notes 1. — Due to the characteristics of synthetic testing it may be difficult to comply with the specified time intervals of the rated operating sequence. See Sub-clause 6.105.1 of IEC Publication 56.

2. — In order to comply with all test requirements it may be necessary to make more operations than provided for in the rated operating sequence. In such cases the circuit-breaker may be reconditioned after the number of operations provided for in the rated operating sequence.

6.106.1
6.106.2 *Test-duties Nos. 1, 2 and 3*
6.106.3

For test-duties Nos. 1, 2, and 3, only breaking tests are specified.

6.106.4 *Test-duty No. 4*

Procedures are known to carry out the rated operating sequence synthetically with the specified parameters (see Table I).

If, due to limitations of the testing station, it is not possible to apply these procedures, the following methods are available:

Method 1

The first breaking operation before the time interval t = 0,3 s or t'' = 15 s may be carried out as an O_D-operation.

The purpose of the additional single breaking test O_s is:

- to comply with the requirement to have two or three breaking operations at specified values,
- to provide the necessary information for the relevant requirements for the setting of the control of the tripping impulse during the subsequent operating sequence.

The conditions of this two-part test are:

- the breaking operation O_D shall be performed under the same arcing time conditions as if direct tests were performed at specified values. Normally, reignition methods (see Appendix JJ) are necessary to achieve this;
- the control of the tripping impulse for the breaking operations of the operating sequence shall be in accordance with the requirements of Sub-clause 6.102.9 (B)1) of IEC Publication 56;
- the setting of the control of the tripping impulse for the single breaking operation O_S shall be such, that the arcing time is the same as for the O_D operation. It may be necessary to make more than one test to realise this.

Methods 2a and 2b

The making and breaking tests may be made separately as test-duties Nos. 4*a* and 4*b* according to Sub-clauses 6.106.4.1 and 6.106.4.2 of IEC Publication 56.

If it is impossible to carry out method 2*a* for circuit-breakers with time intervals t = 0,3 s or t'' = 15 s, method 2*b* can be applied with the first breaking operation O_D and arcing time conditions as specified for method 1.

Closing operations at values of applied voltage lower than those given in Sub-clause 6.104.1 of IEC Publication 56 are only allowed if the requirements of Sub-clause 5.1.1 are fulfilled.

Methods 3a and 3b

If it is not possible to carry out methods 2*a* or 2*b* with making operations at the specified applied voltage, it is under certain conditions permissible (see Sub-clause 5.1.1) to use method 3*a*.

If it is impossible to carry out method 3*a* for circuit-breakers with time intervals t = 0,3 s or t'' = 15 s, method 3*b* can be used with the first breaking operation O_D and arcing time conditions as specified for method 1.

6.106.5 *Test-duty No. 5*

On circuit-breakers having short arcing times three breaking operations shall be made irrespective of the rated operating sequence.

Note. — In order to ensure that the test circuit-breaker is correctly stressed and to establish the minimum arcing time, an extra test may be made. For this test the setting of the control of the tripping impulse has to be as prescribed for the first valid operation, i.e. in or even before the minor loop. The injection of the TRV has to be applied after the minor loop. In this test the test circuit-breaker should reignite. It is important to establish that this reignition has taken place between the arcing contacts only. This demonstrates the voltage withstand co-ordination at dielectric reignitions.

During tests with asymmetrical current both d*i*/d*t* and the TRV are modified due to the d.c. component. In synthetic tests these modifications have to be pre-arranged by:

a) Control of the d.c. component of the current

The d.c. component may be controlled by selection of the point on the wave at which the short-circuit is initiated

b) Reduction of d*i*/d*t* at current-zero

The reduction of d*i*/d*t* may for current injection methods be obtained by reducing the charging voltage of the voltage circuit.

The formula to be applied for the determination of the reduced charging voltage is:

$$U_{HA} = U_{HS}\left[\sqrt{1-p^2} \pm \frac{p}{2\pi f \cdot \tau}\right] \qquad \begin{array}{l} + \text{ for major loop} \\ - \text{ for minor loop} \end{array}$$

where:

U_{HA} = reduced charging voltage at asymmetrical test
U_{HS} = charging voltage for equivalent symmetrical test
p = the per unit value of the d.c. component at current zero
τ = time constant according to IEC Publication 56 (45 ms).

p can be calculated from the asymmetry at contact separation p_{cs}:

$$p = p_{cs} \cdot e - \frac{t_a}{\tau}$$

where:
t_a = arcing time

c) Correction of TRV

1) Simplified method

For TRV's with time t_2 not exceeding 500 µs, a simplified method can be used. This method is based upon the supposition that the correction of TRV (u_1, t_1, u_c, t_2) is proportional to the correction for d*i*/d*t*.

This means that the correction of TRV is automatically covered by the reduced d*i*/d*t* according to *b)*.

2) For TRV's with time t_2 exceeding 500 µs other corrections and/or circuit modifications have to be used. The required prospective TRV values are given in Table II.

Note. — Tables III, IV and V give information with respect to TRV values for a first-pole-to-clear factor of 1.5 and/or a time constant of 120 ms. These values are not IEC Publication 56 ratings. TRV values for time constants other than those given in the tables may be obtained with sufficient accuracy by linear inter and extrapolation, *d)* Correction of recovery voltage

When a test is made for clearance at the end of a major loop the d.c. form of the reduced recovery voltage will adequately cover the first quarter loop of the recovery voltage (of an equivalent direct test).

For clearance at the end of a minor loop of current the d.c. form of the reduced recovery voltage will not cover reference system conditions since in the system the power-frequency recovery voltage continues to rise after the onset of the TRV.

Subject to agreement between testing station, manufacturer and user it may be considered that taken together with the symmetrical test-duties the evidence is sufficient to prove the performance of the circuit-breaker. An asymmetrical test with clearance after a minor loop with reduced d*i*/d*t* and the resulting reduced TRV is assumed to be less severe than an equivalent symmetrical test. However, if it is required to prove fully this test condition, there are three possibilities:

1) the test is performed with asymmetrical current conditions with the voltage source charged as for the symmetrical test. It must be recognised that this represents a considerable increase in severity above that of an equivalent direct test since both d*i*/d*t* and the TRV are higher;

2) the test is performed as under 1) except that the inductance of the injection circuit is increased in inverse proportion to d*i*/d*t*. In this case, the d*i*/d*t* value is correct but the TRV higher;

3) the test is performed with an a.c. recovery voltage.

6.109 *Short-line fault tests*

For short-line fault synthetic testing the parameters of the short-line circuit shall be those given in IEC Publication 56 and the line circuit shall be in the current carrying circuit during the whole interaction interval.

With current injection circuits the short-line circuit may be connected in series with the voltage circuit, its inductance becoming part of L_h e.g. as shown in Figure BB1.

The presence of the short-line fault circuit in the voltage circuit may cause oscillations to be superimposed on the injected current wave. These oscillations should be damped out (to satisfy the requirements of Sub-clause 4.2.1*d*), so as not to affect the current during the interval of significant change of arc-voltage or at least 100 μs before current-zero.

A resistance may be connected in series with the TRV shaping circuit. In most cases this resistance, selected to control the initial rate of rise of recovery voltage, is sufficient to supply the necessary damping.

Note. — If, for short line fault tests, the line is connected to the same side of the test circuit-breaker as the voltage circuit impedance, special attention should be given to voltage distribution and measurement of prospective TRV.

6.111 *Synthetic methods for capacitive-current switching*

See Appendix GG.

TABLE I

Synthetic test sequences for test-duties 1, 2, 3, 4 and 5

Test-duty No.	Synthetic test		Rated operating sequence	
			$O - t - CO - t' - CO$ $t = 0{,}3$ s or 3 min $t' = 3$ min	$CO - t'' - CO$ $t'' = 15$ s
1, 2, 3	Breaking operations*	*a)*	$O_S - t - O_S - t' - O_S$	$O_S - t'' - O_S$
		b)	O_S $O_D - t - O_S - t' - O_S$	O_S $O_D - t'' - O_S$
4	Complete rated operating sequence		$O_S - t - C_SO_S - t' - C_SO_S$	$C_SO_S - t'' - C_SO_S$
	Method 1		O_S $O_D - t - C_SO_S - t' - C_S O_S$	C_SO_S $C_SO_D - t'' - C_SO_S$
	Method 2	*a)*	$C_S - t' - C_S$ $O_S - t - C_DO_S - t' - C_DO_S$	$C_S - t'' - C_S$ $C_DO_S - t'' - C_DO_S$
		b)	$C_S - t' - C_S$ O_S $O_D - t - C_DO_S - t' - C_DO_S$	$C_S - t'' - C_S$ C_DO_S $C_DO_D - t'' - C_DO_S$
	Method 3	*a)*	$O_S - t - C_DO_S - t' - C_DO_S$	$C_DO_S - t'' - C_DO_S$
		b)	O_S $O_D - t - C_DO_S - t' - C_DO_S$	C_DO_S $C_DO_D - t'' - C_DO_S$
5	Breaking operations * **		O_S O_S O_S	

* For convenience in testing, it is permissible to introduce a closing operation before any opening operation in test-duties Nos. 1, 2, 3, and 5.

** For short arcing times only.

TABLE II

TRV after breaking asymmetrical current

Frequency (Hz)		50												60											
Voltage (kV)		245		300		362		420		525		765		245		300		362		420		525		765	
Time co-ordinate (μs)		t_1 130	t_2 390	t_1 159	t_2 477	t_1 192	t_2 576	t_1 223	t_2 669	t_1 279	t_2 837	t_1 406	t_2 1218	t_1 130	t_2 390	t_1 159	t_2 477	t_1 192	t_2 576	t_1 223	t_2 669	t_1 279	t_2 837	t_1 406	t_2 1218
	%	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c
		Voltage (kV)																							
After major-loop: asymmetry at current zero	0	260	364	318	446	384	538	446	624	557	780	812	1137	260	364	318	446	384	538	446	624	557	780	812	1137
	5	260	363	319	445	385	536	446	621	557	775	811	1124	260	363	319	444	384	535	445	620	557	773	810	1121
	10	260	362	318	442	384	532	445	616	556	768	808	1109	260	361	318	441	383	530	444	614	555	764	806	1102
	15	259	359	317	439	382	527	443	610	553	758	804	1091	258	358	316	436	381	525	442	606	551	753	801	1080
	20	257	356	315	434	380	521	440	602	549	747	797	1070	257	354	314	431	378	517	438	597	547	740	793	1055
	25	255	351	312	428	376	514	436	593	543	734	788	1046	254	349	311	424	374	509	434	586	540	724	783	1027
	30	252	346	308	421	371	504	430	581	536	718	776	1019	251	343	307	417	369	498	428	574	533	707	770	996
	35	248	339	303	412	365	494	423	568	527	701	763	988	247	336	302	407	363	487	420	560	523	688	756	962
	40	244	332	298	403	358	481	415	553	517	681	746	954	242	327	296	397	356	473	412	543	512	666	738	925
	45	238	323	291	391	350	467	405	536	504	658	728	916	236	318	289	385	347	458	401	525	499	641	719	883
	50	232	313	283	379	341	451	394	517	490	633	706	875	230	308	280	371	337	441	390	505	484	614	696	838
	55	224	301	274	364	329	433	381	496	474	604	681	829	222	296	271	356	326	422	376	482	467	584	670	788
	60	216	288	263	348	317	413	366	471	455	572	653	778	213	282	260	339	313	401	361	456	448	550	641	733
	65	206	273	251	329	302	390	349	444	433	537	621	721	203	267	248	320	298	377	344	428	426	512	608	673
	70	195	256	238	308	285	364	329	413	408	497	584	658	192	249	234	298	280	350	324	395	400	471	570	607
	75	182	237	222	284	266	334	307	378	380	451	541	587	179	229	218	273	261	319	300	359	371	423	526	532
	80	166	214	203	256	243	299	280	337	346	399	492	506	163	206	198	244	237	284	273	317	337	369	476	447
After minor loop: asymmetric at current zero	0	260	364	318	446	384	538	446	624	557	780	812	1137	260	364	318	446	384	538	446	624	557	780	812	1137
	5	259	364	317	446	383	539	444	626	556	783	811	1146	259	364	318	447	383	540	445	627	556	785	812	1150
	10	257	383	315	445	381	538	442	626	553	785	807	1153	258	364	316	446	381	540	443	628	554	789	809	1160
	15	255	361	313	443	378	536	438	624	549	784	802	1157	256	362	313	445	379	539	440	628	550	790	805	1168
	20	252	358	309	440	373	533	434	621	543	782	795	1158	253	360	310	443	375	537	435	626	545	789	798	1172
	25	249	354	305	435	368	528	428	616	536	777	785	1156	250	356	306	439	370	533	430	622	539	786	790	1174
	30	244	349	299	430	362	522	421	609	527	770	773	1150	245	352	301	434	364	528	423	617	531	781	779	1172
	35	239	343	293	423	355	514	412	601	517	761	759	1142	240	346	295	428	357	521	415	610	521	774	766	1168
	40	233	336	286	414	346	505	402	591	505	750	742	1130	235	340	288	420	349	513	406	601	509	764	750	1159
	45	226	327	278	405	336	494	391	578	491	736	723	1114	228	332	280	411	339	502	395	590	496	752	732	1147
	50	219	318	269	393	325	481	378	564	475	719	700	1094	221	323	271	401	328	490	382	576	481	737	710	1131
	55	210	307	258	380	312	465	364	547	457	699	675	1070	212	313	261	388	316	476	368	561	463	720	686	1111
	60	200	294	246	365	298	448	347	527	437	676	646	1041	203	301	249	374	302	460	352	542	444	698	658	1085
	65	189	280	233	348	282	428	328	504	414	649	613	1007	192	287	236	358	286	441	334	521	421	673	626	1055
	70	177	264	217	329	264	405	307	478	387	618	576	966	179	271	221	339	268	418	313	496	395	644	590	1017
	75	162	245	200	306	243	378	283	448	357	581	533	917	165	252	204	317	248	393	289	467	366	609	548	972
	80	146	223	179	279	218	346	255	412	322	537	483	858	149	231	184	291	224	362	261	432	332	567	499	917

First pole to clear factor 1,3
Time constant of d.c. decrement 45 ms

TABLE III

TRV after breaking asymmetrical current

Frequency	(Hz)	50												60											
Voltage	(kV)	245		300		362		420		525		765		245		300		362		420		525		765	
Time co-ordinate	(µs)	t_1 130	t_2 390	t_1 159	t_2 477	t_1 192	t_2 576	t_1 223	t_2 669	t_1 279	t_2 837	t_1 406	t_2 1218	t_1 130	t_2 390	t_1 159	t_2 477	t_1 192	t_2 576	t_1 223	t_2 669	t_1 279	t_2 837	t_1 406	t_2 1218
	%	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c
		Voltage (kV)																							
After major-loop: asymmetry at current zero	0	260	364	318	446	384	598	446	624	557	780	812	1137	260	364	318	446	384	538	446	624	557	780	812	1137
	5	260	363	318	444	384	535	445	620	554	773	809	1122	260	362	318	443	383	534	445	619	556	772	809	1119
	10	259	360	317	440	382	530	443	614	554	764	805	1104	259	359	317	439	382	528	443	612	553	761	804	1097
	15	257	357	315	436	380	524	440	606	550	753	798	1083	257	356	314	434	379	522	439	603	548	748	796	1073
	20	255	352	312	430	376	516	436	597	544	740	790	1060	255	351	311	428	375	513	435	593	543	734	787	1047
	25	252	347	308	423	372	508	431	586	537	725	779	1033	252	345	308	420	371	504	429	581	535	717	775	1017
	30	249	341	304	415	366	497	424	573	529	708	766	1003	248	339	303	412	365	493	423	567	527	698	761	983
	35	244	334	298	406	359	485	416	559	519	689	750	970	243	331	297	402	358	480	415	551	516	677	745	947
	40	239	325	292	395	352	472	407	542	507	667	732	934	238	322	291	390	350	466	405	534	504	654	727	907
	45	233	316	285	383	343	457	396	524	493	642	712	893	232	312	283	378	341	449	394	515	490	628	705	864
	50	226	305	276	369	332	439	384	504	478	615	688	849	225	301	275	363	330	431	382	493	474	599	681	816
	55	218	292	266	353	320	420	370	481	460	585	662	801	217	288	265	347	318	411	367	469	456	568	654	764
	60	209	279	255	336	307	399	354	455	440	552	631	747	208	274	253	329	304	389	351	442	436	533	623	708
	65	199	263	242	316	291	374	336	426	417	514	597	688	197	258	240	309	288	364	333	413	412	494	588	645
	70	187	245	228	294	273	347	316	394	391	473	559	622	185	240	226	286	271	336	312	379	386	450	549	576
	75	173	225	211	269	253	316	292	357	361	425	514	549	172	219	209	261	250	304	288	342	356	402	504	500
	80	157	202	191	240	229	280	261	315	327	371	463	466	156	195	189	231	226	268	260	299	321	346	452	413
After minor-loop: asymmetric at current zero	0	260	364	318	446	384	538	446	624	557	780	812	1137	260	364	318	446	384	538	446	624	557	780	812	1137
	5	260	365	318	447	384	540	445	627	557	785	812	1149	260	365	318	448	384	541	446	628	557	787	813	1152
	10	259	364	317	447	382	541	444	628	555	788	811	1158	259	365	317	448	383	542	444	630	556	792	812	1185
	15	257	363	315	446	380	540	441	628	552	789	807	1165	257	364	315	448	381	542	442	631	554	794	809	1174
	20	254	361	312	444	377	538	438	626	548	789	802	1168	255	363	313	446	378	541	439	630	549	795	804	1181
	25	251	358	308	440	372	534	433	623	542	786	794	1168	252	360	309	443	373	538	434	628	544	794	797	1185
	30	248	354	304	436	367	529	426	618	534	780	784	1166	248	356	305	439	368	534	428	624	537	790	788	1185
	35	243	348	298	430	360	522	419	611	525	773	771	1160	244	351	299	434	362	528	421	618	528	784	776	1183
	40	238	342	292	422	353	514	410	602	515	763	756	1150	239	345	293	427	354	521	412	610	518	776	762	1177
	45	232	335	284	414	344	504	400	591	502	751	739	1137	233	338	286	419	346	511	402	600	505	765	745	1167
	50	224	326	276	403	333	492	388	578	487	736	718	1120	226	330	277	409	335	500	391	588	491	752	725	1153
	55	216	316	266	391	322	478	374	562	471	718	695	1098	218	320	267	397	324	487	377	573	475	736	703	1134
	60	207	304	254	377	308	462	359	544	452	697	668	1072	206	309	256	384	311	472	362	556	456	716	676	1111
	65	197	290	242	361	293	443	341	522	430	671	637	1040	198	295	244	368	296	454	345	536	435	692	646	1083
	70	185	275	227	347	275	421	321	497	405	642	601	1001	186	280	229	350	278	432	325	512	410	664	611	1047
	75	171	257	210	321	255	396	298	468	376	607	560	955	172	263	213	329	258	407	302	484	381	631	570	1004
	80	155	235	191	295	232	365	271	434	342	565	511	899	157	242	193	304	235	378	275	450	348	590	523	951

First pole to clear factor 1,3
Time constant of d.c. decrement 120 ms

TABLE IV

TRV after breaking asymmetrical current

Frequency (Hz)		50												60											
Voltage (kV)		245		300		362		420		525		765		245		300		362		420		525		765	
Time co-ordinate (µs)		t_1 150	t_2 450	t_1 184	t_2 551	t_1 222	t_2 665	t_1 257	t_2 772	t_1 321	t_2 964	t_1 468	t_2 1405	t_1 150	t_2 450	t_1 184	t_2 551	t_1 222	t_2 665	t_1 257	t_2 772	t_1 321	t_2 964	t_1 468	t_2 1405
	%	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c
		Tension/Voltage (kV)																							
After major loop: asymmetry at current zero	0	300	420	367	514	443	621	514	720	643	900	937	1312	300	420	367	514	443	621	514	720	643	900	937	1312
	5	300	419	368	512	444	618	515	716	643	893	936	1295	300	418	367	512	443	616	514	714	642	890	934	1290
	10	300	417	367	509	443	613	513	710	641	883	932	1274	299	416	366	507	442	611	512	706	640	878	929	1265
	15	299	414	366	505	441	607	511	702	638	871	926	1251	298	412	365	502	439	603	509	697	636	864	922	1236
	20	297	409	363	453	438	599	507	692	633	857	917	1224	296	407	362	495	436	594	505	685	630	847	912	1205
	25	294	404	360	492	433	590	502	680	626	840	906	1193	293	401	358	487	431	583	499	672	622	828	900	1169
	30	290	397	355	483	428	578	495	666	617	821	893	1159	289	393	353	478	425	571	492	656	613	807	885	1130
	35	286	390	350	473	421	565	487	650	607	800	877	1121	284	385	347	467	418	557	484	639	602	783	868	1088
	40	281	380	343	461	413	551	478	632	594	775	858	1080	279	375	340	454	409	541	474	619	589	756	848	1041
	45	274	370	335	448	403	534	466	612	580	748	835	1033	272	364	332	440	399	522	462	597	574	726	824	990
	50	267	358	326	433	392	515	453	589	563	717	810	983	264	352	323	424	388	502	448	573	556	693	798	935
	55	258	345	315	416	379	493	438	563	544	683	781	927	256	337	312	406	374	479	433	545	536	657	767	874
	60	249	329	303	396	364	469	421	534	522	645	748	865	246	321	299	385	359	454	415	515	514	616	733	808
	65	237	312	289	375	347	442	401	502	497	603	710	797	234	303	285	363	342	426	394	481	488	572	694	735
	70	224	292	273	350	328	411	378	466	468	556	667	722	221	283	269	337	322	394	371	443	458	522	650	655
	75	209	269	255	321	305	376	352	424	435	502	618	638	205	259	250	308	299	357	344	400	424	466	599	566
	80	191	243	233	288	279	336	321	376	396	440	560	542	187	232	228	274	272	316	313	350	385	402	540	465
After minor loop: asymmetric at current zero	0	300	420	367	514	443	621	514	720	643	900	937	1312	300	420	367	514	443	621	514	720	643	900	937	1312
	5	299	420	366	515	442	622	513	723	642	905	936	1325	299	421	367	516	442	623	513	724	642	908	937	1330
	10	297	419	364	514	440	622	510	724	638	908	933	1336	298	420	365	516	440	625	511	727	640	913	935	1345
	15	295	417	381	512	436	621	506	722	634	909	927	1343	295	419	362	515	437	624	508	727	636	916	930	1357
	20	291	414	357	509	431	617	501	720	627	907	919	1347	292	416	358	513	433	622	503	726	630	917	924	1366
	25	287	410	352	504	425	612	494	715	619	903	908	1347	288	413	354	509	427	619	497	723	623	915	914	1371
	30	282	404	346	498	418	606	486	708	609	896	895	1343	283	408	348	504	421	613	489	718	614	911	902	1372
	35	276	397	339	491	410	597	476	699	598	887	879	1336	278	402	341	497	413	606	480	710	603	904	887	1370
	40	269	390	331	482	400	587	465	688	584	875	860	1325	271	395	333	489	403	597	469	701	590	894	870	1363
	45	262	380	321	471	389	575	452	674	568	860	838	1309	264	386	324	479	393	586	457	689	575	882	849	1353
	50	253	369	311	458	376	560	438	658	550	842	813	1289	255	376	314	467	380	573	443	675	557	866	825	1337
	55	243	357	298	443	362	544	421	640	530	820	784	1264	246	364	302	454	366	557	427	568	538	847	798	1317
	60	232	343	285	427	345	524	402	618	507	795	751	1233	235	351	289	438	350	539	408	637	515	824	766	1291
	65	219	327	269	407	327	501	381	593	480	765	714	1196	222	335	273	419	332	518	387	614	489	796	730	1259
	70	204	308	252	385	306	475	356	563	450	730	671	1151	208	317	256	398	311	493	364	586	460	764	689	1219
	75	188	286	232	359	281	445	329	529	416	689	622	1098	192	296	236	373	288	464	336	553	426	725	641	1170
	80	169	261	208	329	253	409	296	488	375	640	564	1032	173	272	213	343	260	429	304	514	387	678	584	1109

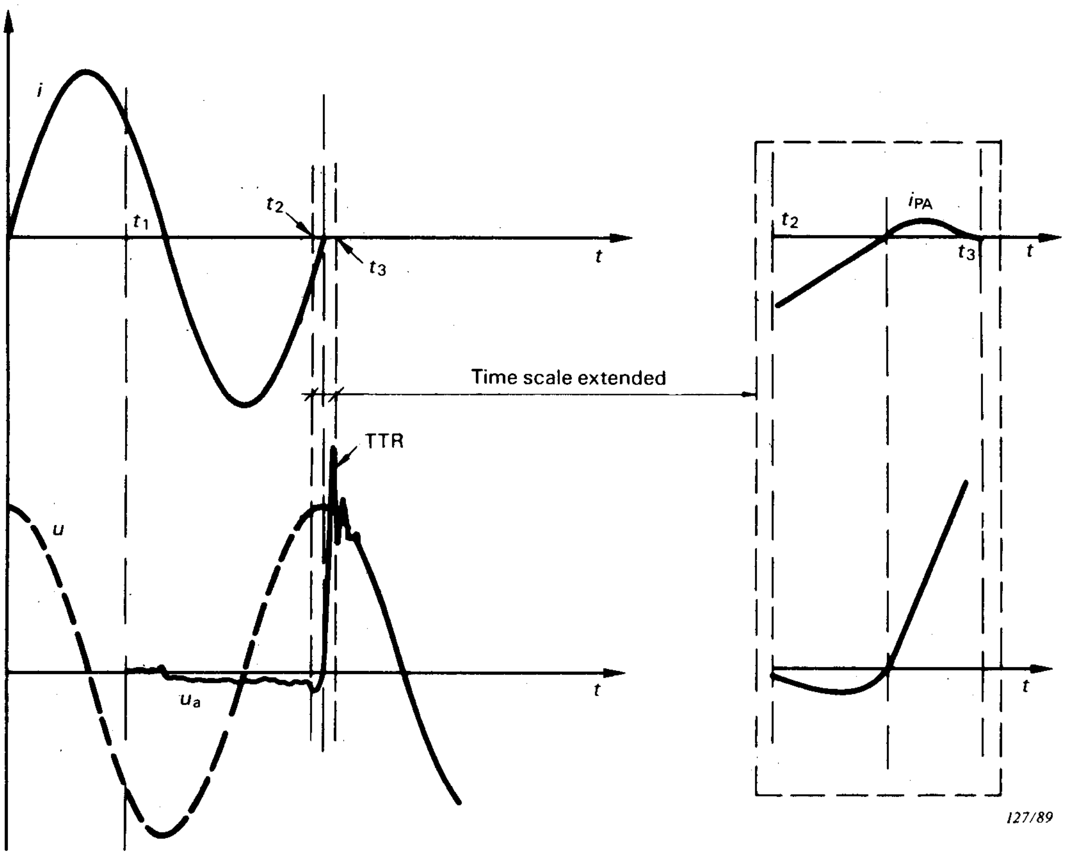
First pole to clear factor: 1.5
Time constant of d.c. decrement: 45 ms

TABLE V

TRV after breaking asymmetrical current

Frequency (Hz)		50												60											
Voltage (kV)		245		300		362		420		525		765		245		300		362		420		525		765	
Time co-ordinate (μs)		t_1 150	t_2 450	t_1 184	t_2 551	t_1 222	t_2 665	t_1 257	t_2 772	t_1 321	t_2 964	t_1 468	t_2 1405	t_1 150	t_2 450	t_1 184	t_2 551	t_1 222	t_2 665	t_1 257	t_2 772	t_1 321	t_2 954	t_1 458	t_2 1405
	%	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c
		Voltage (kV)																							
After major loop: asymmetry at current zero	0	300	420	367	514	443	621	514	720	643	900	937	1312	300	420	367	514	443	621	514	720	643	900	937	1312
	5	300	418	367	511	443	616	513	714	641	891	934	1292	300	418	367	511	442	615	513	713	641	889	933	1287
	10	299	415	365	507	441	610	511	706	638	879	928	1269	298	414	365	506	440	608	510	704	637	875	926	1260
	15	297	411	363	501	438	603	507	697	633	865	920	1242	296	409	363	499	437	600	507	693	632	859	917	1229
	20	294	406	360	494	434	594	503	685	627	849	909	1212	294	404	359	492	433	589	501	680	625	841	906	1195
	25	291	399	356	486	428	583	496	672	619	830	896	1179	290	397	355	482	427	578	495	665	616	820	892	1157
	30	287	392	350	476	422	570	489	657	609	809	881	1141	286	389	349	472	420	564	487	648	606	797	875	1115
	35	281	383	344	465	414	556	479	639	597	786	862	1101	280	380	343	460	412	549	477	630	594	771	856	1070
	40	275	373	336	452	405	540	469	619	583	759	841	1056	274	369	335	446	403	531	466	608	579	742	834	1021
	45	268	362	328	438	394	521	456	597	567	730	817	1007	267	357	326	431	392	512	453	585	563	711	809	967
	50	260	349	318	422	382	501	442	573	549	697	789	953	259	344	316	414	380	491	439	559	544	676	780	909
	55	251	334	306	403	368	478	426	546	529	661	758	894	250	329	304	395	365	467	422	531	523	638	748	846
	60	241	318	293	383	352	453	407	515	505	621	723	830	239	312	291	374	349	440	403	499	500	596	712	777
	65	229	300	279	360	335	424	386	481	479	577	683	759	227	293	276	350	331	411	382	464	473	550	672	702
	70	215	279	262	334	314	392	362	443	448	528	638	681	213	272	259	324	311	378	358	424	442	498	626	619
	75	199	255	242	304	290	356	335	400	414	472	587	593	197	248	240	293	287	340	330	380	407	441	573	528
	80	181	228	220	270	263	314	303	351	373	408	527	494	179	220	217	259	259	297	298	329	366	375	512	424
After minor loop: asymmetric at current zero	0	300	420	367	514	443	621	514	720	643	900	937	1312	300	420	367	514	443	621	514	720	643	900	937	1312
	5	300	421	367	516	443	624	514	724	643	907	938	1328	300	422	367	517	443	625	514	726	643	909	939	1333
	10	298	421	366	517	442	625	513	727	641	912	937	1342	299	422	366	518	442	627	513	729	642	916	938	1350
	15	297	420	363	516	439	625	510	727	638	915	933	1352	297	421	364	518	440	628	511	731	639	921	936	1365
	20	294	418	360	514	435	623	505	726	633	915	927	1358	294	420	361	516	436	627	507	731	635	923	930	1376
	25	290	414	356	510	430	619	500	723	626	913	918	1362	291	417	357	514	431	624	501	729	629	923	923	1383
	30	286	410	351	505	424	614	493	717	618	908	907	1361	287	413	352	509	426	620	495	726	621	921	912	1387
	35	281	404	344	499	417	607	484	710	608	901	893	1357	282	407	346	504	418	614	487	720	611	916	899	1387
	40	275	397	337	491	408	598	474	701	595	891	876	1349	276	401	339	496	410	606	477	712	599	908	884	1384
	45	268	389	329	481	398	587	463	689	581	878	857	1336	269	393	330	487	400	597	465	701	585	897	865	1375
	50	259	379	319	469	386	574	449	674	565	862	833	1319	261	384	321	477	388	584	452	688	569	883	842	1363
	55	250	367	307	456	372	559	434	657	545	842	807	1297	252	373	309	464	375	570	437	672	551	865	817	1345
	60	240	354	294	440	357	540	416	637	524	819	776	1269	241	360	297	449	360	553	420	653	529	844	787	1321
	65	227	339	280	422	339	519	396	613	499	791	741	1235	229	345	282	431	343	533	400	631	505	818	752	1291
	70	214	321	263	401	319	494	372	585	470	758	700	1193	216	328	266	411	323	509	377	604	477	787	713	1254
	75	198	300	244	376	296	465	346	552	437	719	653	1142	200	308	246	387	300	481	350	573	444	750	666	1208
	80	179	276	221	347	269	431	314	513	398	672	598	1080	182	284	224	359	273	447	320	535	406	705	612	1150

First pole to clear factor: 1,5
Time constant of d.c. decrement 120 ms



t_2 = start of significant change in arc voltage

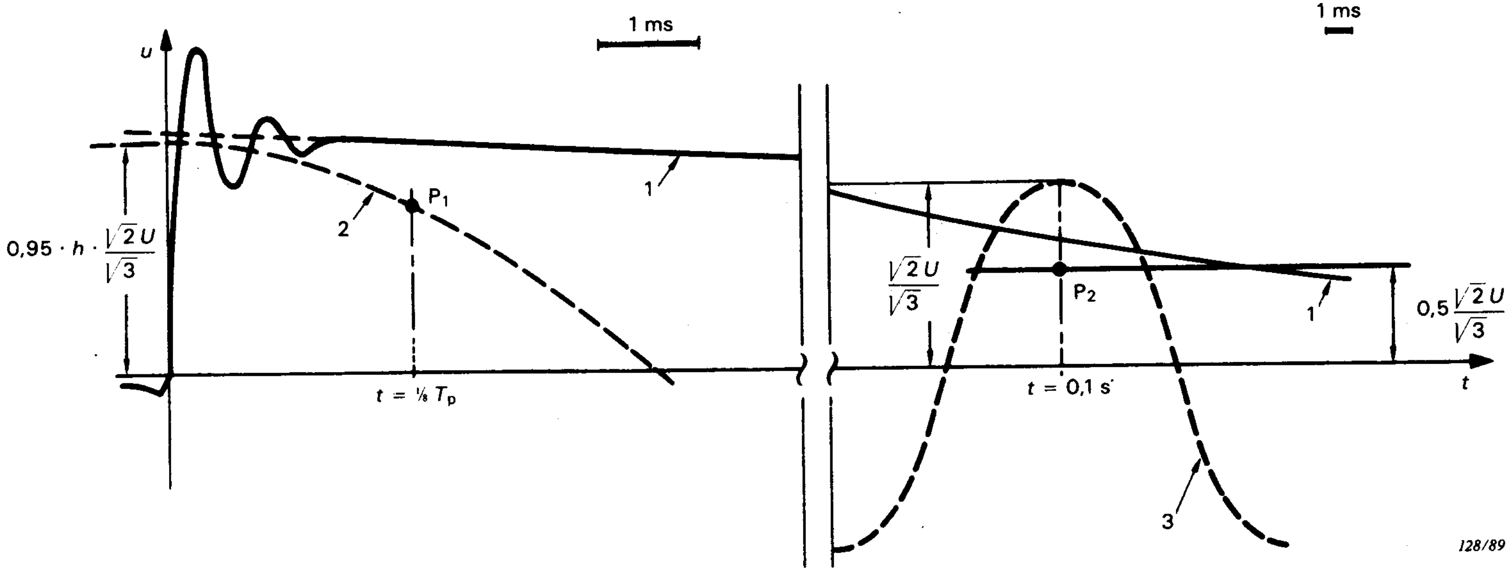
t_3 = instant of cessation of post-arc current

$t_2 - t_1$ = high-current interval

$t_3 - t_2$ = interaction interval

After t_3 = high-voltage interval

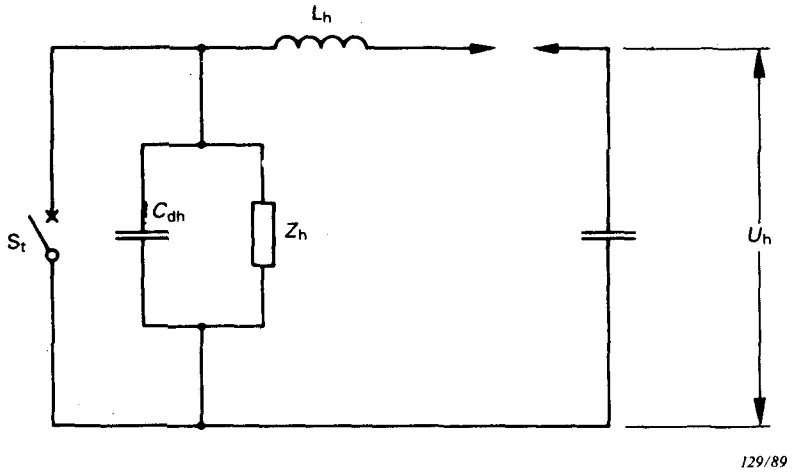
FIG. 1. — Interrupting process; basic time intervals.



P_1 = point to which the recovery-voltage (1) shall not fall below the specified value (2)

P_2 = point below which the recovery-voltage (1) shall not fall during a synthetic test

T_p = power frequency period.



U_h = charging voltage of voltage circuit

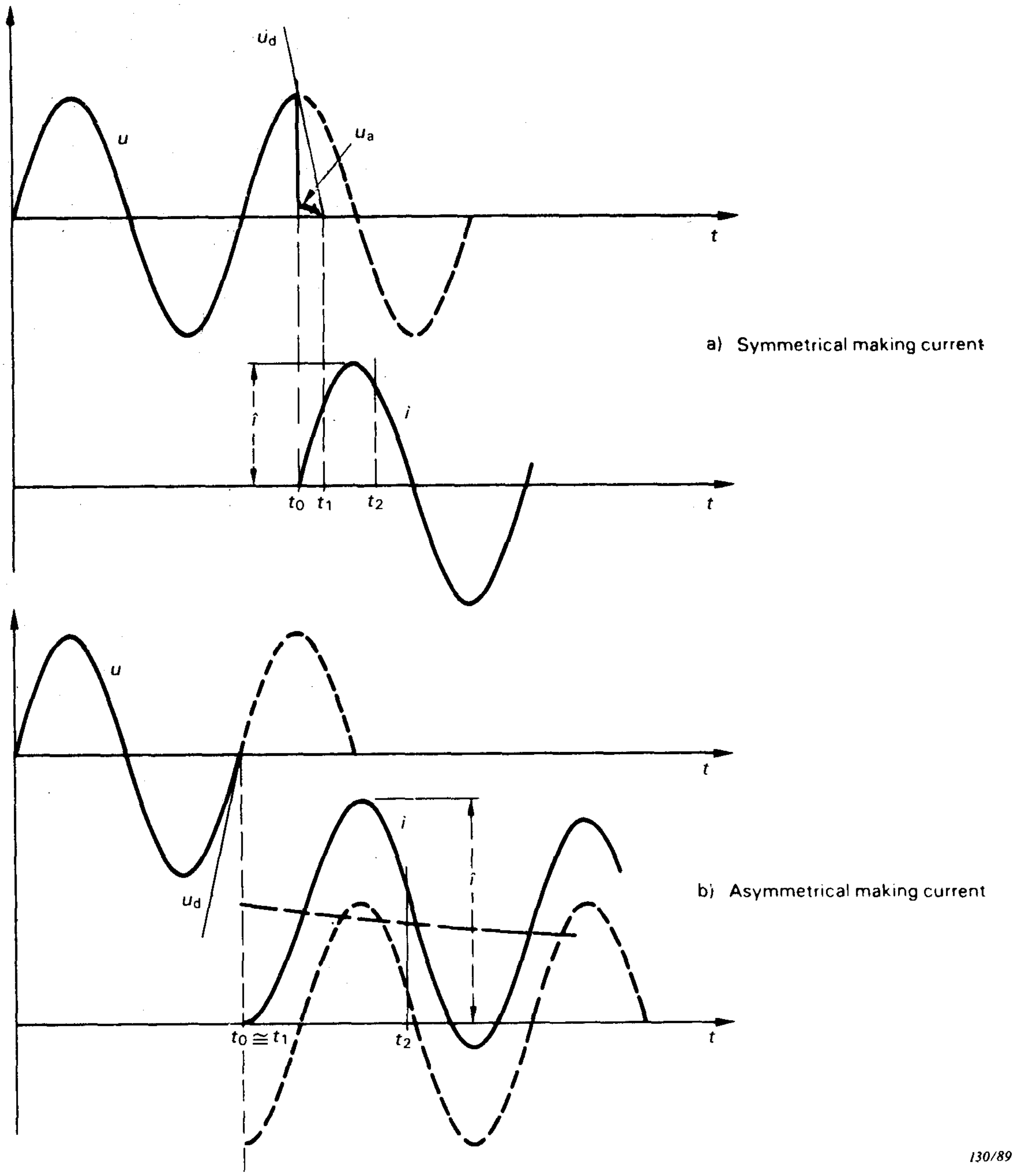
L_h = inductance of voltage circuit

Z_h = equivalent surge impedance

C_{dh} = capacitance for time delay of voltage circuit

S_t = test circuit-breaker

FIG. 3.— Equivalent surge impedance within the voltage circuit of current injection scheme.



= current

= making current peak

= power-frequency voltage

= dielectric closing characteristic

= arc-voltage

Time intervals:

Before t_0 = high-voltage interval

$t_0 - t_1$ = pre-arcing interval

$t_1 - t_2$ = latching interval

After t_2 = fully closed position

FIG. 4.— Making process: basic time intervals.

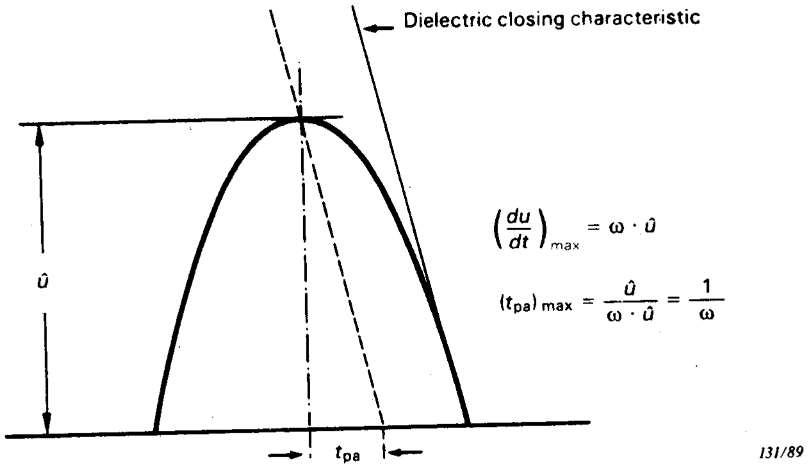
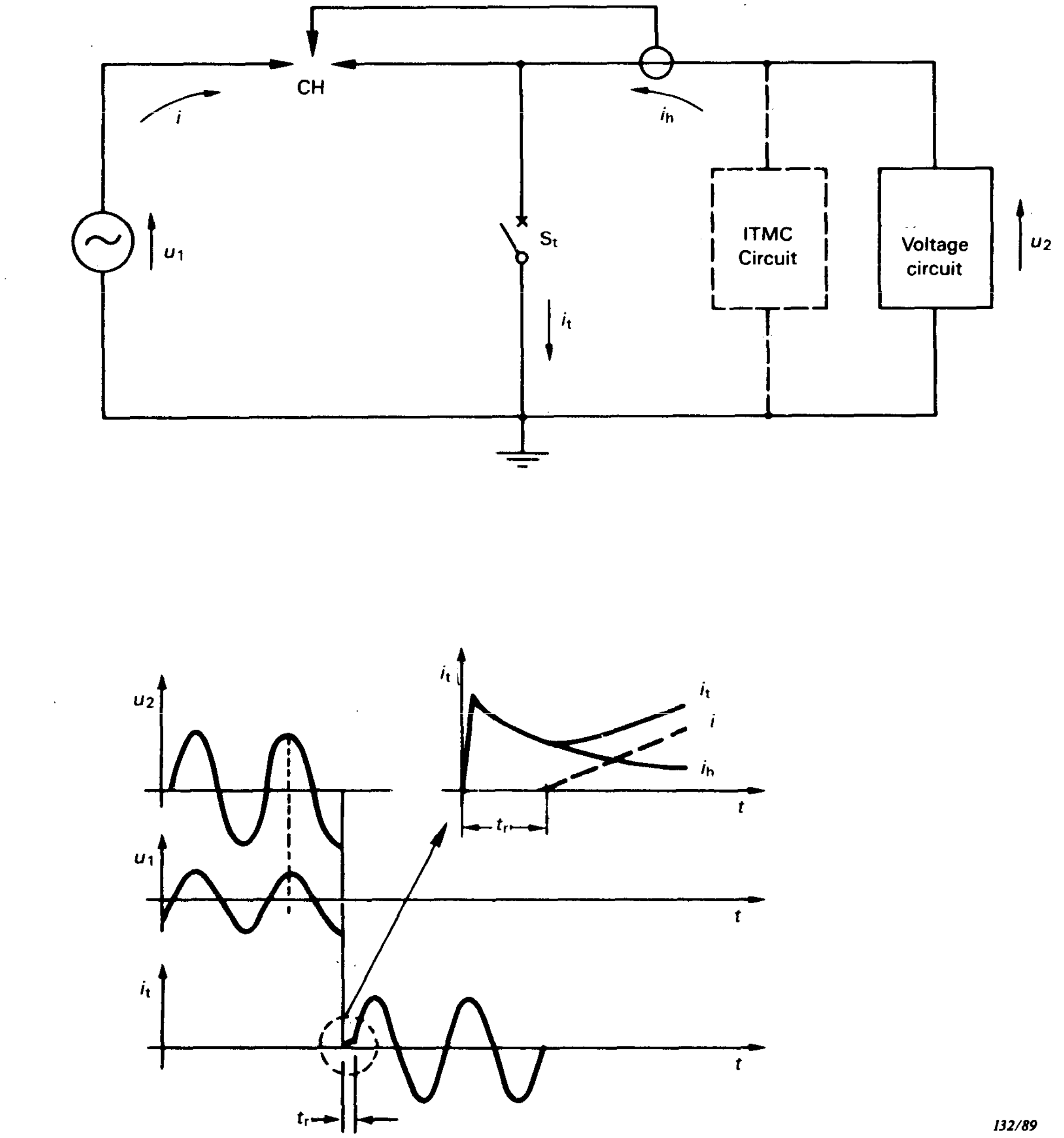

Dielectric closing characteristic
$\hat{u}$
$\left(\frac{du}{dt}\right)_{max} = \omega \cdot \hat{u}$
$(t_{pa})_{max} = \frac{\hat{u}}{\omega \cdot \hat{u}} = \frac{1}{\omega}$
t_{pa}
131/89

FIG. 5.— Maximum allowable pre-arcing time for valid making test at reduced voltage.



u_1 = voltage of current circuit

CH = making device (triggered spark gap)

i = power-frequency current supplied by current circuit

= test circuit breaker

u_2 = applied voltage

i_h = initial transient making current (ITMC)

i_t = current in the test circuit-breaker

t_r = time delay of making device

FIG. 6.— Synthetic make circuit and waveforms.

APPENDIX AA

CURRENT DISTORTION

AA1. Current distortion immediately prior to current-zero

The interaction interval begins when the arc-voltage starts to change significantly as the current approaches zero. The change of the arc-voltage during this time influences the shape and the rate-of-change of the current immediately before current-zero.

This deviation from the prospective current curve is caused by the distortion current, which mainly flows in the low time constant impedance, taking into account all parameters of the actual circuit.

The particular way in which the current approaches zero is responsible for the conditions prevailing between the arcing-contacts of a circuit-breaker at current-zero particularly for the conditions which exist in the medium between the arcing-contacts. The major interaction between circuit and circuit-breaker is caused by the arc-voltage charging and discharging capacitances and influencing d*i*/d*t* just before zero.

In a simplified circuit, as in Figure AA1a representing a short-circuit in service or a direct test, the voltage u supplies an arc-current i with the appropriate arc-voltage u_a. Parallel to the arc is a capacitor C.

If it is assumed that the arc-voltage $u_a = 0$, then a prospective short-circuit current i_p (see Figure AA1b) will flow through the arc, the magnitude and wave shape of this current being determined by the inductance L, the voltage u, the frequency of this voltage and the moment of current initiation.

If it is assumed that the supply voltage $u = 0$ and that an arc-voltage exists, then the arc-voltage will produce a current flow. This current i_d (see Figure AA1c) is the distortion current, which will flow partly as i_{dL} through the inductance L, and partly as i_{dC} through the capacitance C. For this condition, the following equations apply:

$$u_a - L \cdot \frac{d}{dt}(i_{dL}) = 0$$

and

$$C \frac{d}{dt}(u_a) - i_{dC} = 0$$

From these, the following equation for i_d can be obtained:

$$i_d = i_{dL} + i_{dC} = \frac{1}{L}\int u_a dt + C \cdot \frac{d}{dt}(u_a)$$

If both of the voltages, u and u_a are present (see Figure AA1d), then the resulting actual current is given by:

$$i = i_p - i_d$$

Note. — For actual cases digital calculations by computers may be more appropriate where various arc-voltage wave shapes can be introduced.

AA2. Current distortion during the high current interval

During this interval, the arc-voltage generates a distortion current i_d, in the circuit. i_d is superimposed on the total current.

By comparison with the prospective current, the resulting arc current exhibits distortion in four physical aspects: current amplitude, loop duration, arc-energy and di/dt.

To evaluate the influence of the arc-voltage it is sufficient, in practice, to consider the current amplitude and the loop duration.

As a first approximation, two different arc-voltage characteristics can be considered, namely:

1) a constant arc-voltage $u_a = U_a$
2) a linearly rising arc-voltage $u_a = S \cdot t$

Since the current through the capacitor C (see Figure AA1a) will be small during this period of arcing, the simplified diagram of Figure AA2a is adequate.

AA2.1 *Distortion during one loop of arcing related to a symmetrical current*

The following formulae are derived, where the resistance in Figure AA2a is neglected since the effect of this during the single loop is negligible. Some results are given in Figure AA3a and AA3b.

Calculations are made based on the characteristics shown in Figure AA2b and AA2c.

$\hat{u} = L \cdot \omega \cdot \hat{i}_p$ = peak value of voltage of current circuit
$\hat{i}_p$ = peak value of prospective current
$\hat{i}$ = peak value of actual current (reduced by arc-voltage)
t_m = instant of peak value $\hat{i}$

a) Ratio of current amplitudes

— for constant arc-voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin \omega \cdot t_m - \frac{U_a}{\hat{u}} \cdot \omega \, t_m$$

— for linearly rising arc-voltage:

$$\frac{\hat{i}}{\hat{i}_p} = \sin \omega \cdot t_m - \frac{S\omega}{2\,\hat{u}} \, t_m^2$$

b) Actual current loop duration T_l (reduced by arc-voltage)

— for constant arc-voltage :

$$\sin \omega \, T_l = \frac{U_a \, \omega}{\hat{u}} T_l$$

— for linearly rising arc-voltage:

$$\sin \omega \, T_l = \frac{S\omega}{2\,\hat{u}} T_l^2$$

In Figure AA3a, and AA3b relative reduction of current amplitude $\Delta i/\hat{i}_p$ and current loop duration $\Delta t/T_p$ are given as a function of ratio $U_a/\hat{u}$ for constant arc-voltage and of ratio $S \cdot T_a/2 \cdot \hat{u}$ for linearly rising arc-voltage respectively, where:

$\Delta i = \hat{i}_p - \hat{i}$
$\Delta t = T_p - T_l$

T_p = prospective current loop duration
T_a = actual arcing time ($T_a = T_l$ for one loop of arcing, see Figures AA2b and AA2c).

AA2.2 *Distortion in general case*

The distortion currents in the case of both symmetrical and asymmetrical currents including more than one loop of arcing are obtained by the following formulae which are applicable for the case of constant and linearly rising arc-voltages. These calculations are based on a circuit as in Figure AA2a where the L/R time constant of the supply impedance is introduced. The p.u. prospective current is given by:

$$i_p/\hat{i}_p = \sin(\omega t + \omega t_l - \varphi) - \sin(\omega t_l - \varphi) \cdot e^{-\frac{R}{L}t}$$

where:

t = time coordinate counting from the instant of current initiation
t_l = time interval between the beginning of the positive voltage loop and current initiation

$\varphi = \arctan \frac{\omega L}{R}$ For symmetrical current $\varphi = \omega t_l$

The per unit distortion currents are:

$i_d/\hat{i}_p = C$ for the first loop of arcing
$i_d/\hat{i}_p = D - E$ for the second loop of arcing
$i_d/\hat{i}_p = D - F + G$ for the third loop of arcing

where:

C, D, E, F and G are defined as follows:

a) for constant arc-voltage:

$$C = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t_{cs})}\right]$$

$$D = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t'_o - t_{cs})}\right] e^{-\frac{R}{L}(t - t'_o)}$$

$$E = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t'_o)}\right]$$

$$F = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t''_o - t'_o)}\right] e^{-\frac{R}{L}(t - t''_o)}$$

$$G = \frac{M}{\cos\varphi}\left[1 - e^{-\frac{R}{L}(t - t''_o)}\right]$$

where:

$M = \dfrac{U_a}{\hat{u}}$ = the ratio between the arc-voltage and the peak value of the power-frequency voltage

$\cos\varphi = \dfrac{R}{\sqrt{R^2 + (\omega L)^2}}$

t_{cs} = instant of contact separation
t'_o, t''_o = instants at the end of each current loop

b) for linearly rising arc-voltage:

$$C = \frac{M}{\cos\varphi} \left[(t - t_{cs}) - \frac{L}{R} \left(1 - e^{-\frac{R}{L}(t - t_{cs})}\right) \right]$$

$$D = \frac{M}{\cos\varphi} \left[(t'_o - t_{cs}) - \frac{L}{R} \left(1 - e^{-\frac{R}{L}(t'_o - t_{cs})}\right) \right] e^{-\frac{R}{L}(t - t'_o)}$$

$$E = \frac{M}{\cos\varphi} \left[(t - t'_o) - \frac{L}{R} \left(1 - e^{-\frac{R}{L}(t - t'_o)}\right) + (t'_o - t_{cs}) \cdot \left(1 - e^{-\frac{R}{L}(t - t'_o)}\right) \right]$$

$$F = \frac{M}{\cos\varphi} \left[(t''_o - t'_o) - \frac{L}{R} \left(1 - e^{-\frac{R}{L}(t''_o - t'_o)}\right) \right.$$
$$\left. + (t'_o - t_{cs}) \cdot \left(1 - e^{-\frac{R}{L}(t''_o - t'_o)}\right) \right] e^{-\frac{R}{L}(t - t''_o)}$$

$$G = \frac{M}{\cos\varphi} \left[(t - t''_o) - \frac{L}{R} \left(1 - e^{-\frac{R}{L}(t - t''_o)}\right) + (t''_o - t_{cs}) \cdot \left(1 - e^{-\frac{R}{L}(t - t''_o)}\right) \right]$$

Where:

$M = \dfrac{S \cdot T_a}{2\hat{u}}$

Relative reductions of current amplitudes and loop durations related to the last arcing loop for some typical cases are given in Figures AA3a to AA3d.

For symmetrical current, values are given for constant arc-voltage as a function of ratio $U_a/\hat{u}$ in Figure AA3a and for linearly rising arc-voltage as a function of the ratio $S \cdot T_a/2\hat{u}$ in Figure AA3b. For asymmetrical current the corresponding results are given in Figures AA3c and AA3d.

For arcing times, three typical values, i.e. for one, two and two and half loops, are introduced. In the case of asymmetrical current contact parting positions have been selected starting about 1.5 cycles after current initiation.

The modifying of arc-voltage is much dependent on not only arc-voltage but also arcing time and current asymmetry, therefore an exact evaluation for each case is necessary.

Note. — In order to be able to compare the curves relevant to either type of arcing suitable values have been chosen for the arc-voltages: the value at the last current zero for linearly rising arc-voltage is twice the value U_a for the constant arc-voltage.

AA3. Examples of estimation of the parameters of the distorted current

In the following, some examples of application of the methods of evaluation of the distorted current shown in the preceding clauses AA1 and AA2 are given for the single pole test of a 123 kV circuit-breaker.

For the synthetic test examples, equal arc-voltages and contact parting positions of both the test and the auxiliary circuit-breaker are assumed.

AA3.1 *Symmetrical current test*

AA3.1.1 *Constant arc-voltage*

Direct test

Rated voltage $U = 123$ kV

Single pole test voltage $U_t = \dfrac{123 \cdot 1{,}3}{\sqrt{3}} = 92$ kV

Mean value of constant arc-voltage (last loop) $U_a = 1$ kV

Therefore: $\dfrac{U_a}{\hat{u}} = \dfrac{1}{92 \cdot \sqrt{2}} = 0{,}0077$

by calculation for one loop of arcing (see Sub-clause AA2.1): $\dfrac{\Delta i}{\hat{\imath}_p} = -\ 1{,}2\%$

and: $\dfrac{\Delta t}{T_p} = -\ 0{,}7\%$

Synthetic test

Current circuit voltage $U_l = 31$ kV

Mean value of constant arc-voltage (test and auxiliary circuit-breaker, last loop) $U_{as} = 2 . U_a = 2$ kV

therefore: $\dfrac{U_{as}}{\hat{u}} = \dfrac{2}{31 \cdot \sqrt{2}} = 0{,}046$

from Figure AA3a for one loop of arcing $\dfrac{\Delta_i}{\hat{\imath}_p} = -7\%$

and: $$\frac{\Delta t}{T_p} = -4{,}5\%$$

AA3.1.2 *Linearly rising arc-voltage*

Direct test

Single pole test voltage $U_t = 92$ kV as above

Linearly rising arc-voltage $$\frac{S\,T_a}{2} = 3 \text{ kv}$$

therefore: $$\frac{S\,T_a}{2\,\hat{u}} = \frac{3}{92\sqrt{2}} = 0{,}023$$

from Figure AA3b for one loop of arcing $$\frac{\Delta i}{\hat{\imath}_p} = -1{,}7\%$$

and: $$\frac{\Delta t}{T_p} = -2{,}2\%$$

Synthetic test

Current circuit voltage $U_{\mathrm{I}} = 31$ kV as above

Linearly rising arc-voltage (test and auxiliary circuit-breaker) $$\frac{S\,T_a}{2} = 2 \cdot 3 \text{ kV} = 6 \text{ kV}$$

therefore: $$\frac{S\,T_a}{2\,\hat{u}} = \frac{6}{31\sqrt{2}} = 0{,}137$$

from Figure AA3b for one loop of arcing $$\frac{\Delta i}{\hat{\imath}_p} = -10\%$$

and: $$\frac{\Delta t}{T_p} = -11{,}2\%$$

In the first example, the tolerances on the amplitude and the duration of the power-frequency current loop, according to Sub-clause 4.1, should not be exceeded during the actual synthetic test. This depends, however, on the decrement of the a.c. component of the current being negligible.

In the second example, the current circuit voltage has to be increased or other measures as described in Sub-clause 4.1 have to be taken because the tolerance on the loop duration is exceeded. Whilst tolerance on the current amplitude is apparently not exceeded, it might be exceeded in practice where there is likely to be some decrement of the a.c. component of the prospective current.

AA3.2 *Asymmetrical current test*

If the arc-voltage is approximately constant or linearly rising, the curves in Figures AA3c and AA3d can be used. The method of evaluation is similar to the one outlined for the symmetrical case. For example in case of constant arc-voltage:

Direct test

Single pole test voltage $$U_t = \frac{123 \cdot 1,3}{\sqrt{3}} = 92 \text{ kV}$$ (as above)

Constant arc-voltage $$U_a = 1 \text{ kV}$$

therefore: $$\frac{U_a}{\hat{u}} = \frac{1}{92 \cdot \sqrt{2}} = 0,0077$$

for contact parting at around 1,5 cycle after current initiation and one loop of arcing $$\frac{\Delta i}{\hat{i}_p} = -1\%$$

and: $$\frac{\Delta t}{T_p} = -0,6\%$$ (Figure AA3c)

Synthetic test

Current circuit voltage $$U_1 = 14,2 \text{ kV}$$
Constant arc-voltage (test and auxiliary circuit-breakers) $$U_a = 2 \text{ kV}$$

therefore: $$\frac{U_a}{\hat{u}} = \frac{2}{14,2\sqrt{2}} = 0.10$$

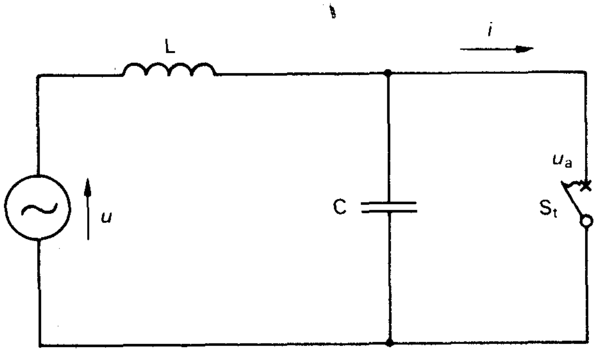
for the same situation as above: $$\frac{\Delta i}{\hat{i}_p} = -12,6\%$$

and: $$\frac{\Delta t}{T_p} = -8,0\%$$ (Figure AA3c)

The actual arc-voltage may not follow one of the simplified characteristics. In such a case the current reduction during the synthetic test can be measured from actual oscillograms or calculated. The actual current of the direct test which is required to establish the synthetic test driving voltage can only be calculated.

For circuit-breakers having relatively low arc-voltage (e.g. $U_a = 2\% \, U_1$), the modifying effect of the arc-voltage on the current in the system or in the direct circuit is negligible. Therefore the specified prospective current is assumed as reference current.

Note. — If the opening of the auxiliary circuit-breaker is delayed in relation to the opening of the test circuit-breaker or if an auxiliary circuit-breaker with a lower arc-voltage is used, then its influence on the breaking current will be smaller than that of the test circuit-breaker.



u = voltage supplying the direct circuit

u_a = arc-voltage of circuit-breaker

L = inductance of the full power direct circuit, together with u controlling the short-circuit current

C = capacitance of the full power direct circuit, together with L controlling the transient recovery-voltage of the circuit

S_t = circuit-breaker

i = arc-current

FIG. AA1a. — Direct circuit, simplified diagram.

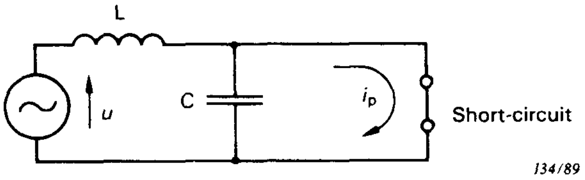


FIG. AA1b. — Prospective short-circuit current.

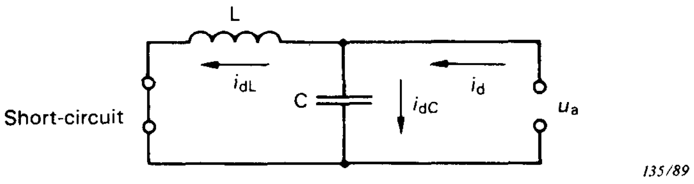


FIG. AA1c. — Distortion current.

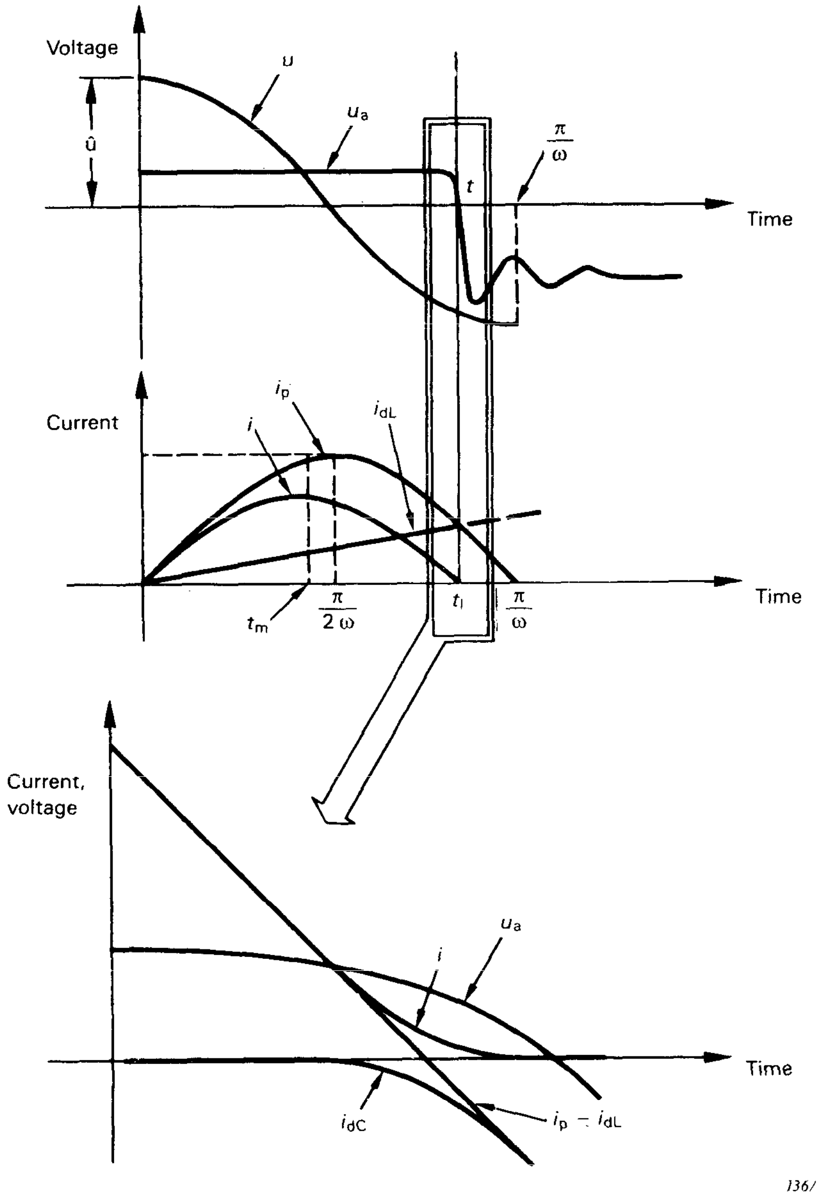


FIG. AA1d. — Distortion current.

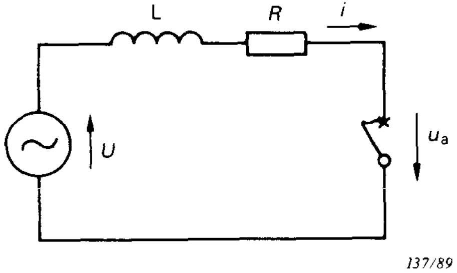


FIG. AA2a. — Simplified circuit diagram.

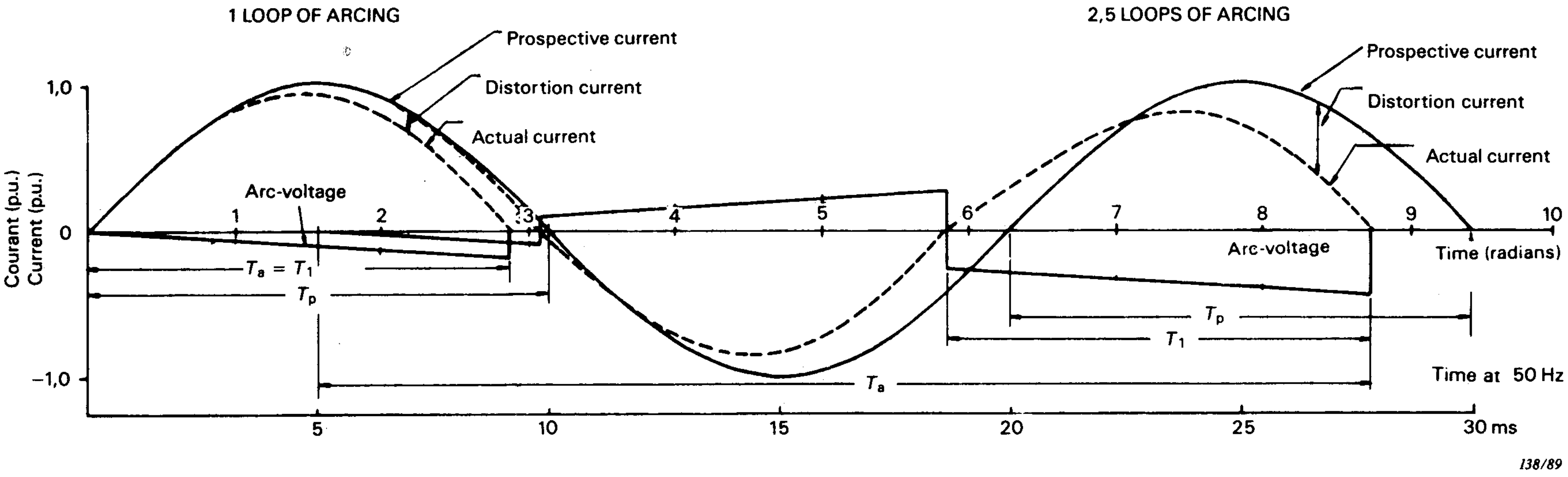


FIG. AA2b. — Current and arc-voltage characteristics for symmetrical current.

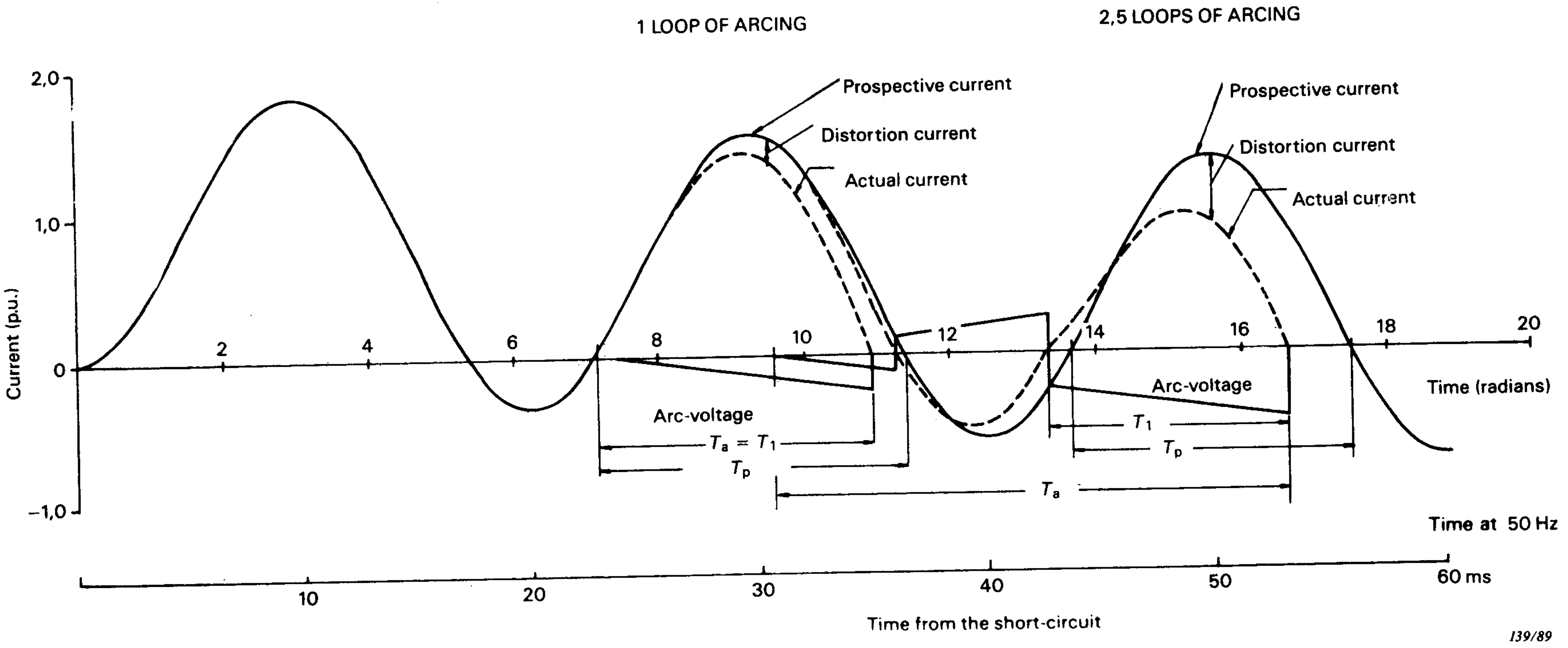
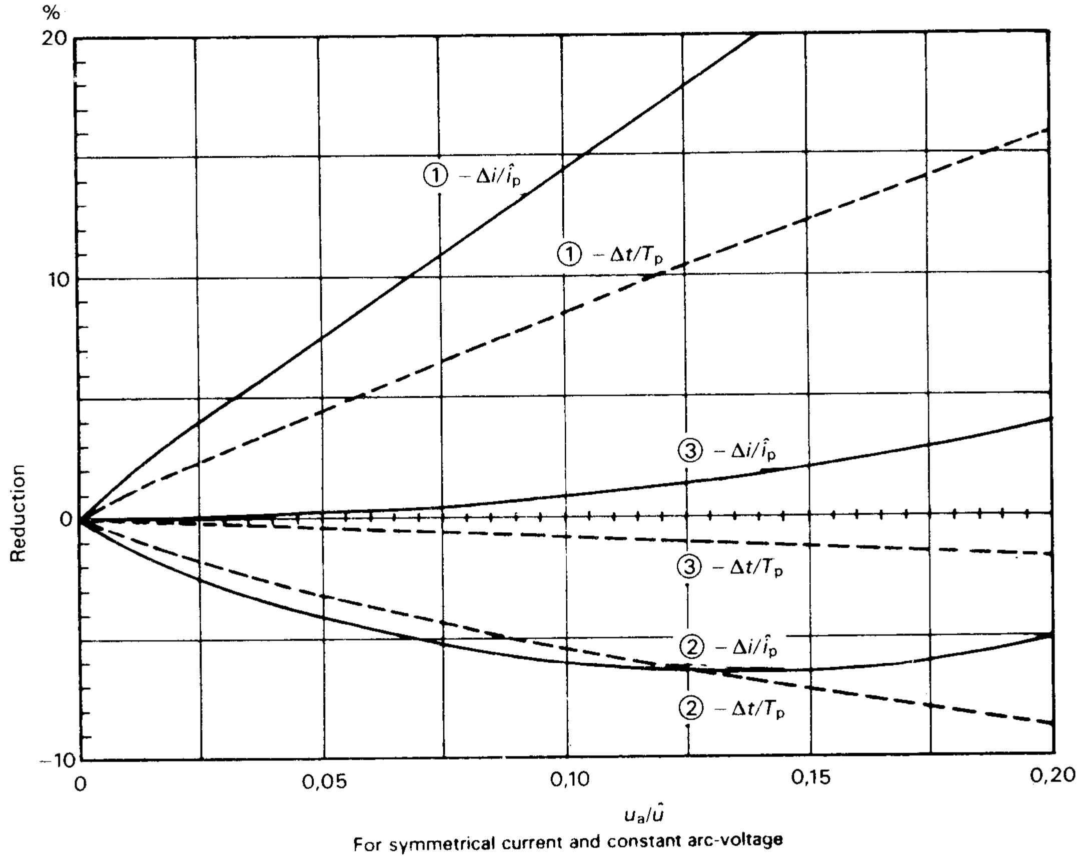


FIG. AA2c. — Current and arc-voltage characteristics for asymmetrical current.



140/89

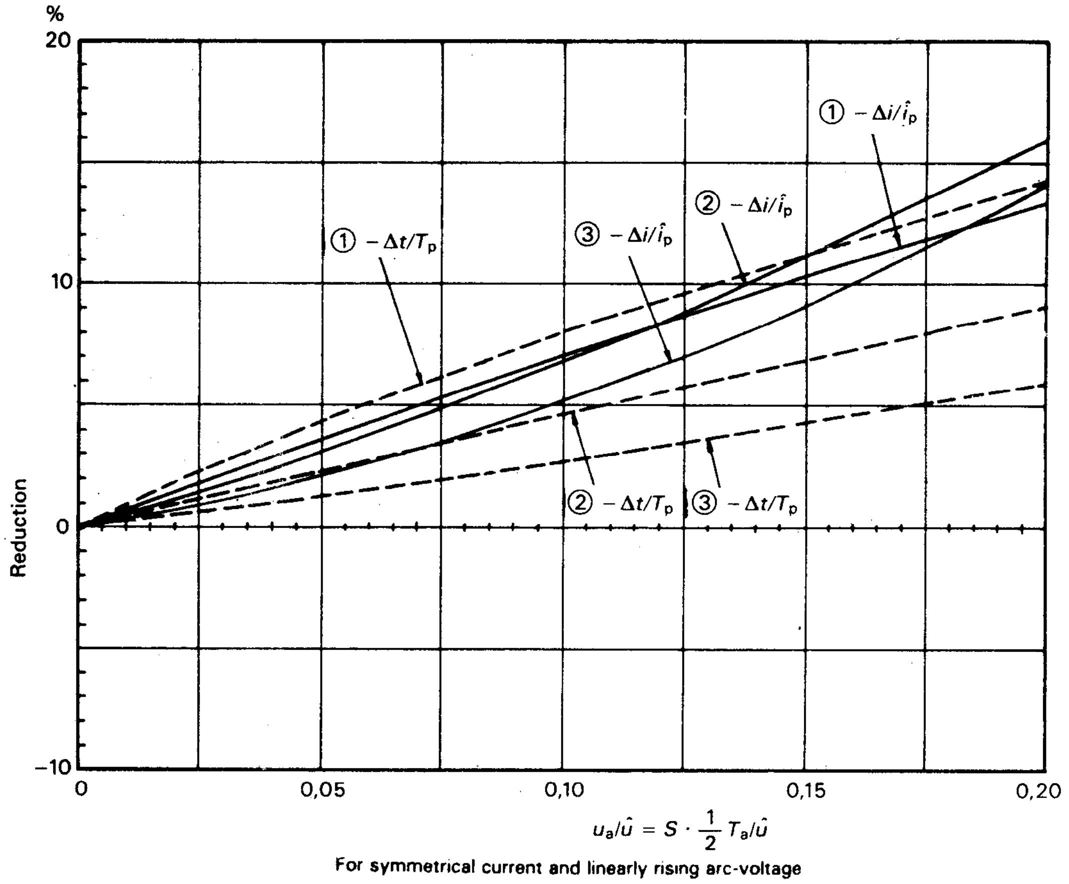
① — 1 loop of arcing

② — 2 loops of arcing

③ — 2,5 loops of arcing

See figure AA2b

FIG. AA3a. — Reduction of amplitude and duration of final current loop of arcing.



141/89

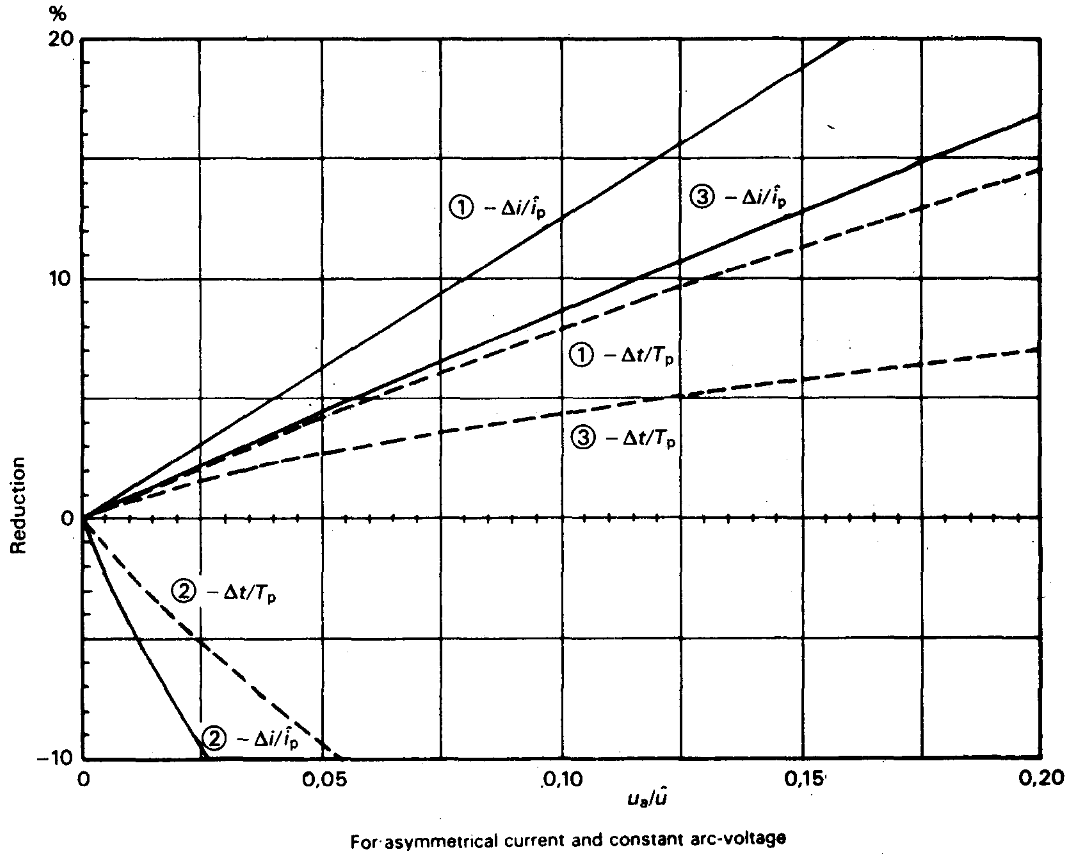
① — 1 loop of arcing

③ — 2,5 loops of arcing

② — 2 loops of arcing

See figure AA2b

FIG. AA3b. — Reduction of amplitude and duration of final current loop of arcing.



142/89

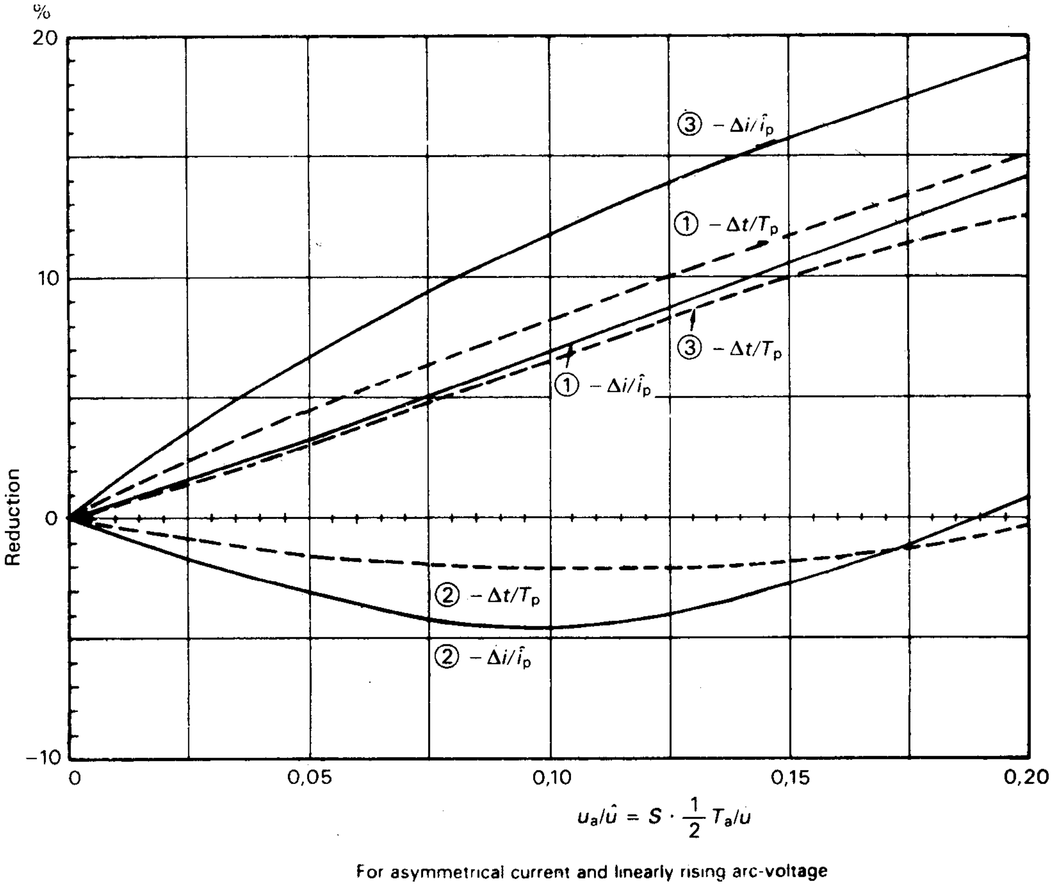
① — 1 loop of arcing

② — 2 loops of arcing

③ — 2,5 loops of arcing

See figure AA2c

FIG. AA3c. — Reduction of amplitude and duration of final current loop of arcing.



143/89

① — 1 loop of arcing

③ — 2,5 loops of arcing

② — 2 loops of arcing

See figure AA2c

FIG. AA3d. — Reduction of amplitude and duration of final current loop of arcing.

APPENDIX BB

CURRENT INJECTION METHODS

BB1. **Current injection**

In a synthetic test circuit using current injection, the superposition of the currents takes place shortly before the zero of the power-frequency short-circuit current. A current of smaller amplitude but higher frequency, derived from the voltage circuit, is superimposed either in the test circuit-breaker or in the auxiliary circuit-breaker. The instant of switching in this injected current is selected by means of a current-dependent control circuit. This instant should be such that the character of the resulting current wave in the test circuit-breaker corresponds to that of the specified breaking current prior to the current-zero during the interval of significant change of arc-voltage.

In this way, the circuit-breaker under test is automatically connected into the voltage circuit after the interruption of the current in the auxiliary circuit-breaker, so there will be no delay between the current stress and the application of the voltage stress.

BB.1.1 *Current injection circuit with the voltage circuit in parallel with the test circuit-breaker (parallel circuit)*

Figure BB1 shows the simplified circuit diagram of a current injection circuit with the voltage circuit connected in parallel with the test circuit-breaker.

The voltage circuit is switched in shortly before the zero of the power-frequency short-circuit current, prior to the interaction interval. At this time the high-frequency oscillatory current i_h is superimposed on the power-frequency short-circuit current i, with the same polarity, to give a resultant test current in the test circuit-breaker.

After the auxiliary circuit-breaker interrupts the power-frequency short-circuit current i, the test circuit breaker is connected only to the voltage circuit and i_h is the only remaining current. The voltage circuit also provides the recovery voltage across the test circuit-breaker after the current is interrupted.

Figure BB2 shows an example of injection timing. The two points of inflection typically indicate the start of the current injection in the test circuit-breaker and the interruption of the power-frequency short-circuit current by the auxiliary circuit-breaker. The waveshape of the transient recovery voltage can be adjusted by varying Z_h and C_{dh} (Figure BB1), to obtain compliance with the requirements of IEC Publication 56 (see Sub-clause 4.1.3).

BB1.2 *Current injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit)*

Figure BB3 shows the simplified circuit diagram of a current injection circuit with the voltage circuit connected in parallel with the auxiliary circuit-breaker.

After switching in the voltage circuit, shortly before the zero of the power frequency short-circuit current, the high-frequency oscillatory current i_h is superimposed, with opposing polarity, on the power-frequency short-circuit current i, in the auxiliary circuit-breaker.

After the resulting current in the auxiliary circuit-breaker has ceased to flow, the oscillatory current commutates into the test circuit-breaker and the current circuit. The test circuit-breaker is now part of a circuit which comprises the series-connected current circuit and the voltage circuit. After the extinction of the resulting current in the test circuit-breaker, the transient recovery voltage is supplied both by the voltage circuit and the current circuit.

Figure BB4 shows an example of injection timing. The single point of inflection corresponds to the interruption of current in the auxiliary circuit-breaker.

The waveshape of the recovery voltage can be adjusted by varying Z_h and C_{dh} as well as Z_l and C_{dl} (Figure BB3) to obtain compliance with the requirements of IEC Publication 56 (see Sub-clause 4.1.3).

BB2. Determination of the interval of significant change of the arc-voltage

To determine the interval of significant change of the arc-voltage which occurs immediately prior to current-zero, the following method may be applied dependent on individual arc-voltage characteristics.

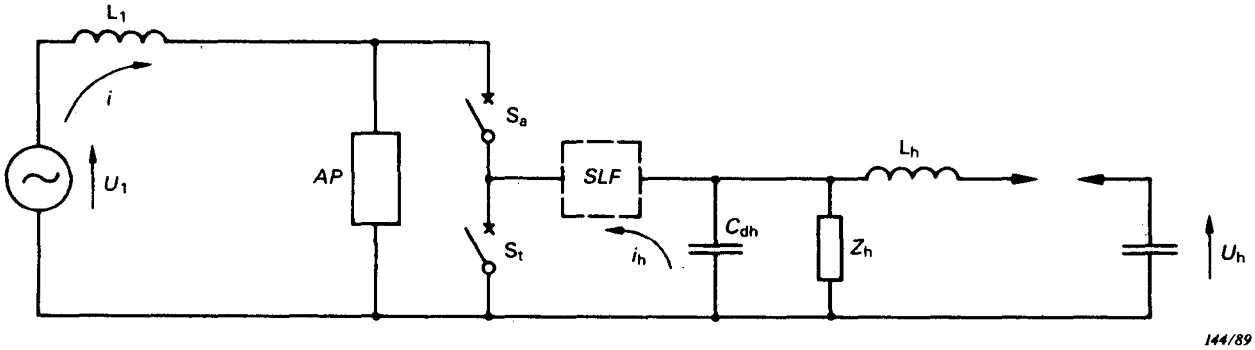
The arc-voltages of circuit-breakers vary considerably in general shape. In many cases, the arc-voltage is not steady but fluctuates about a mean value. For the purpose of identifying a significant change, a mean value is obtained by drawing a smooth curve between the maximums and minimums (Figure BB5). The shape of mean arc-voltage characteristics may also vary widely.

Most circuit-breakers show a nearly constant or steadily rising arc-voltage during the current loop, with an appreciable increase just prior to current-zero. In such cases, it is not difficult to determine from the oscillogram the instant at which a significant change begins. For this purpose, it is preferable to use an oscillograph giving a relatively large deflection for the arc-voltage and having a time scale which is fast enough to enable the interval of significant change of arc-voltage to be measured accurately.

In some cases, it may be difficult to determine the interval of significant change of arc-voltage because:

1) the arc-voltage remains nearly constant or is steadily rising during the current loop almost to the instant of current-zero;
2) changes in the arc-voltage occur considerably before the current-zero.

In these cases, an injection current frequency as low as possible shall be used, taking account also of the requirements in Sub-clause 4.2.1.



U_1 = voltage of current circuit

L_1 = inductance of current circuit

AP = arc prolonging circuit

S_a = auxiliary circuit-breaker

S_t = test circuit-breaker

Z_h = equivalent surge impedance of voltage circuit

C_{dh} = capacitance for time delay of voltage circuit

L_h = inductance of voltage circuit

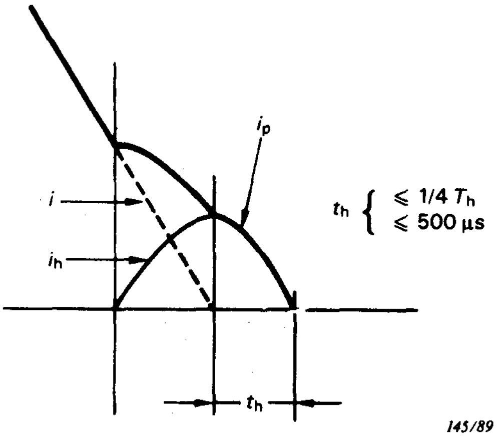
U_h = charging voltage of voltage circuit

i = current of the current circuit

i_h = injected current

SLF = short-line-fault circuit (for the corresponding tests)

FIG. BB1. — Typical current injection circuit with voltage circuit in parallel with the test circuit-breaker.



i = current in the auxiliary circuit-breaker

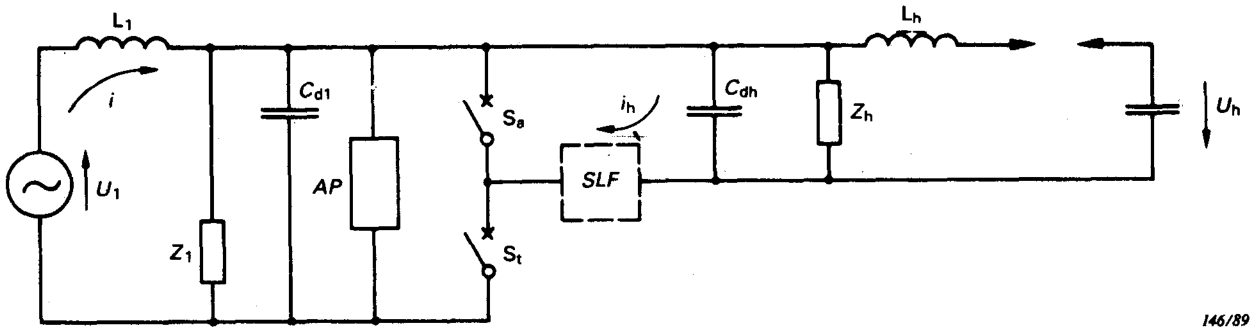
i_h = injected current

i_p = current in the test circuit-breaker

T_h = duration of one period of the injected current

t_h = time during which the arc is fed only by the injected current

FIG. BB2. — Injection timing for current injection scheme with circuit BB1.



U_1 = voltage of current circuit

L_1 = inductance of current circuit

AP = arc prolonging circuit

S_1 = auxiliary circuit-breaker

S_a = test circuit-breaker

Z_h = equivalent surge impedance of voltage circuit

C_{dh} = capacitance for time delay of voltage circuit

L_h = inductance of voltage circuit

U_h = charging voltage of voltage circuit

i = current of the current circuit

i_h = injected current

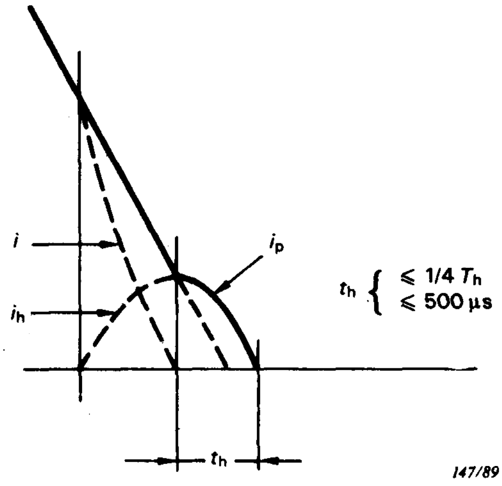
Z_1 = equivalent surge impedance of current circuit

C_{d1} = capacitance for time delay of current circuit

capacitance f

SLF = short-line-fault circuit (for the corresponding tests)

FIG. BB3. — Typical current injection circuit with voltage circuit in parallel with the auxiliary circuit-breaker.



i = current in the auxiliary circuit-breaker

i_h = injected current

i_p = current in the test circuit-breaker

t_h = time during which the arc is fed only by the injected current

FIG. BB4. — Injection timing for current injection scheme with circuit BB3.

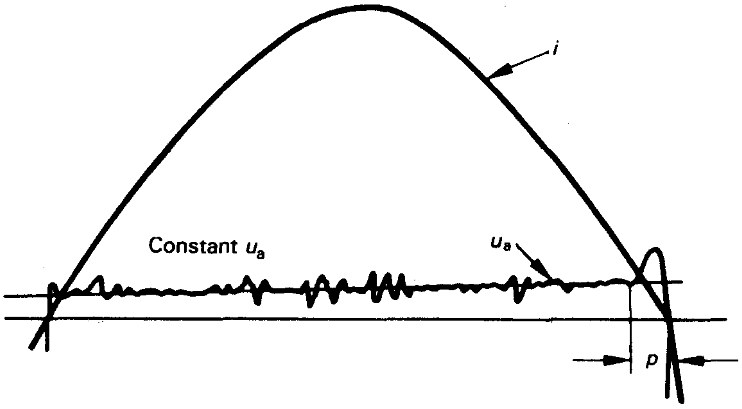


Figure BB5a

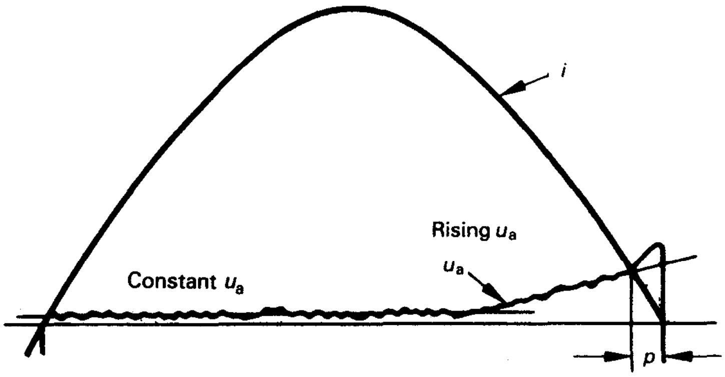


Figure BB5b

i = current

u_a = arc-voltage

p = interval of significant change of arc-voltage

FIG. BB5. — Examples of the determination of the interval of significant change of arc-voltage from the oscillograms.

APPENDIX CC

VOLTAGE INJECTION METHODS

In a synthetic test circuit using voltage injection, the current circuit provides the entire short-circuit current for the test circuit-breaker and also, after current-zero, the first part of the transient recovery voltage.

By suitable choices of its voltage and natural frequency, the correct values of the power factor, current and first part of the TRV can be obtained.

About the time of the first peak of the transient recovery voltage of the current circuit, the voltage circuit is switched in by means of a voltage dependent control circuit in such a way that the specified transient recovery voltage is continued and so that there will be no delay between the current stress and the voltage stress.

CC1. Voltage injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit)

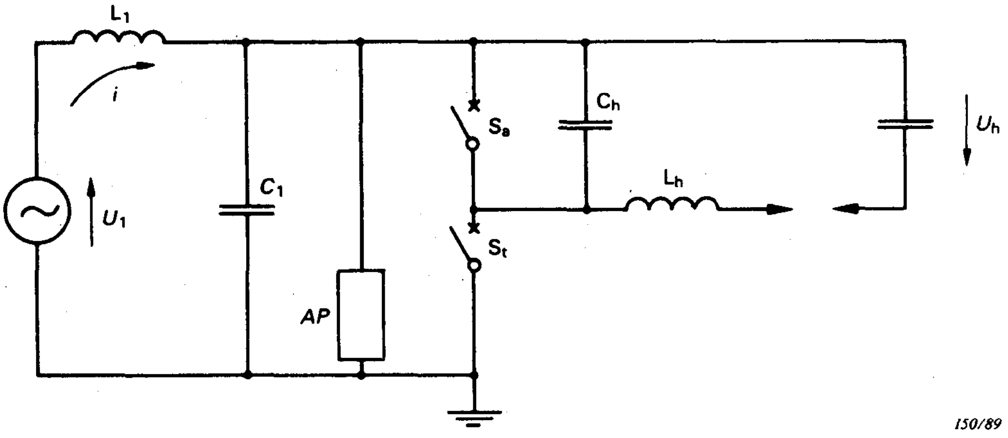
Figure CC1 shows the simplified circuit diagram of a voltage injection circuit with the voltage circuit connected in parallel with the auxiliary circuit-breaker. The current circuit supplies the entire short-circuit current stress. A capacitor of suitable value is connected in parallel with the auxiliary circuit-breaker. After the current-zero of the power-frequency short-circuit current, this capacitor transmits the entire transient recovery voltage of the current circuit to the test circuit-breaker, passing the necessary energy for the post-arc current.

About the time of the first peak of this transient voltage, the voltage circuit will be switched in and from this moment onwards the transient recovery voltages of both circuits are added together to form the transient recovery voltage across the test circuit-breaker.

Figure CC2 shows the current in the test circuit-breaker and the waveshape of the voltage across the auxiliary circuit-breaker and test circuit-breaker. The auxiliary circuit-breaker is stressed only by the voltage of the voltage circuit. Both components of the voltage across the test circuit-breaker are superimposed to produce the transient recovery voltage, the waveshape of which can be adjusted by varying C_h and C_l in conjunction with additional components—not shown in Figure CC1—to obtain compliance with the requirements of IEC Publication 56 (see Sub-clause 4.1.3).

CC2. Voltage injection circuit with the voltage circuit in parallel with the test circuit-breaker

This voltage injection circuit is similar to the one described above except that the voltage circuit is in parallel with the test circuit-breaker instead of the auxiliary circuit-breaker. It is not in common usage.



U_I = voltage of current circuit

L_I = inductance of current circuit

C_I = capacitance of current circuit which together with L_I controls the first part of the TRV

AP = arc prolonging circuit

S_a = auxiliary circuit-breaker

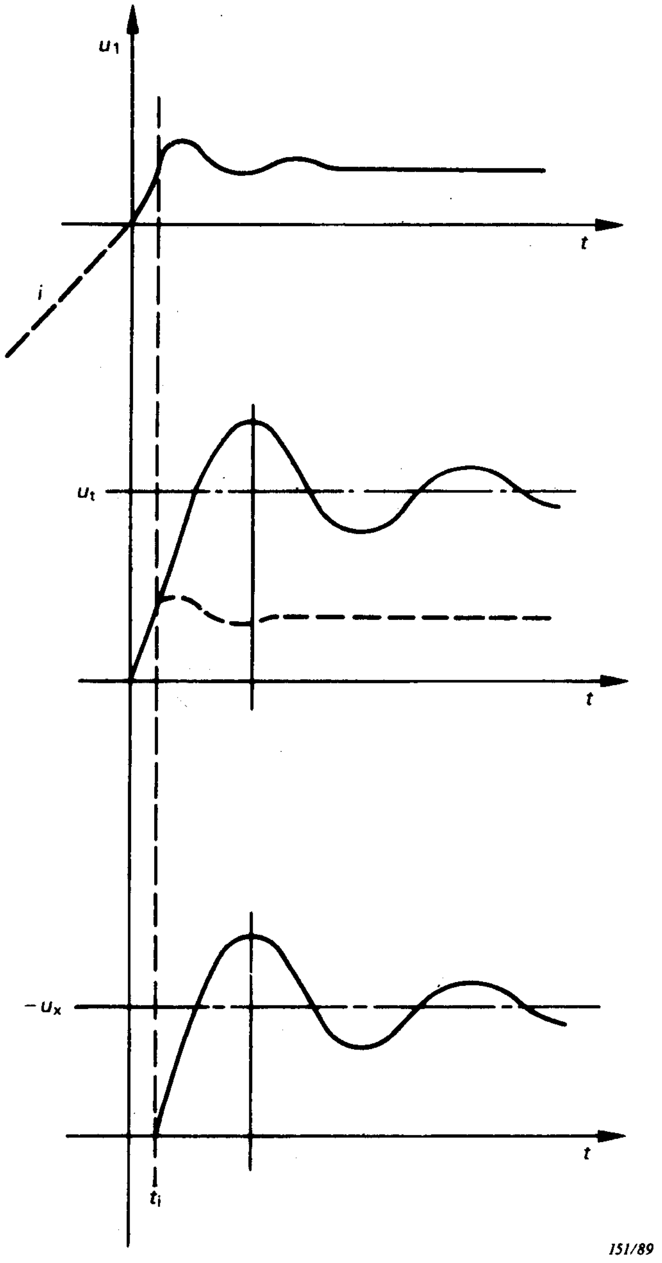
S_t = test circuit-breaker

C_h = capacitance of voltage circuit which together with L_h controls the major part of the TRV

L_h = inductance of voltage circuit

U_h = charging voltage of voltage circuit

FIG. CC1. — **Typical voltage injection circuit diagram with voltage circuit in parallel with the auxiliary circuit-breaker (simplified diagram).**



i = power-frequency current in test and auxiliary circuit-breakers

u_1 = TRV from current circuit

u_t = voltage across test circuit-breaker

u_x = voltage across auxiliary circuit-breaker

t_i = instant of voltage injection

FIG. CC2. — TRV waveshapes in a voltage injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker.

APPENDIX DD

DUPLICATE CIRCUIT (TRANSFORMER OR SKEATS CIRCUIT)

DD1. Principle of the method

In the duplicate test circuit the current is supplied from a current circuit to the series combination of the auxiliary and the test circuit-breaker. The high voltage is applied to the test circuit-breaker via a resistance from a transformer (or auto-transformer) the primary of which is connected to the current circuit across the auxiliary and test circuit-breakers. Figure DD1 shows the principal lay-out of the circuit.

During the high current interval the arc-voltages of the test and auxiliary circuit-breakers induce a current, i_R in the high-voltage circuit which adds to the current through the test circuit-breaker, $i_2 = i_1 + i_R$. The current in the auxiliary breaker will thus reach zero and interrupt before the test circuit-breaker. If the arc-voltages are assumed nearly constant the test circuit-breaker current will go through zero a time Δt after the interruption of the auxiliary breaker approximately given by:

$$\Delta t = \frac{n\,(u_{al} + u_{at}) - u_{at}}{n \cdot \hat{u}_1} \cdot \frac{L_2}{R}$$

where:

n = transformer ratio
u_{al}, u_{at} = arc-voltages in S_l and S_t respectively
u_1 = voltage of current circuit
L_2 = $n^2 . L_1 + L_T$ (effective inductance in the high-voltage circuit)
L_T = leakage inductance of T

During the interval Δt, the rate of change of the current through the test circuit-breaker di_2/dt will approximately attain the value:

$$\frac{di_2}{dt} = - \frac{n \cdot \hat{u}_1}{.L_2} = - \frac{n\,\hat{u}_1}{n^2\,L_1 + L_T}$$

i.e. di_2/dt will be lower than the prospective uninfluenced value. This value is reduced by a factor of the same magnitude as the transformer ratio n.

By choosing the resistance, R, sufficiently large, the time interval Δt could be kept small. On the other hand a high value will increase the damping of the TRV. For circuit-breakers with post-arc current the value may be further restricted. Values of R in the range some kilohms are normally used giving $\Delta t \leqslant 10$ µs.

The test circuit is thus not valid for tests where attention is paid to the thermal failure mode of a circuit-breaker, because:

- the source-side impedance does not correspond to network (or direct test circuit) conditions during the interaction interval;
- the di/dt deviates from the prospective value during a (short) time interval just before current-zero.

The test circuit could be used when testing the dielectric recovery of a circuit-breaker. It could further be used for closing tests and could be extended to work with several full voltage applications.

DD2. Practical arrangement of the circuit

A practical circuit arrangement is shown in Figure DD2. It could be used to apply full recovery voltage in three consecutive current-zeros in an opening operation by opening the auxiliary circuit-breakers S_1, S_2 and S_3 in turn. The spark gaps G_1 and G_2 are triggered to restore the current if the test circuit-breaker fails to interrupt in the first and second current-zero respectively.

It can also apply full voltage stresses at both closing and opening in a CO operation. The test circuit-breaker, S_t, closes against full voltage (S_1 is open) and, when it pre-strikes, one of the spark gaps, e.g. G_2, is triggered to make the current circuit (S_3 is closed). S_1 is closed before the opening of the test circuit-breaker and used as auxiliary circuit-breaker at the first current-zero. If necessary a second current-zero could be tested by means of G_1 and S_2.

In the same way the two opening operations in an auto-reclosing operation could be fully tested.

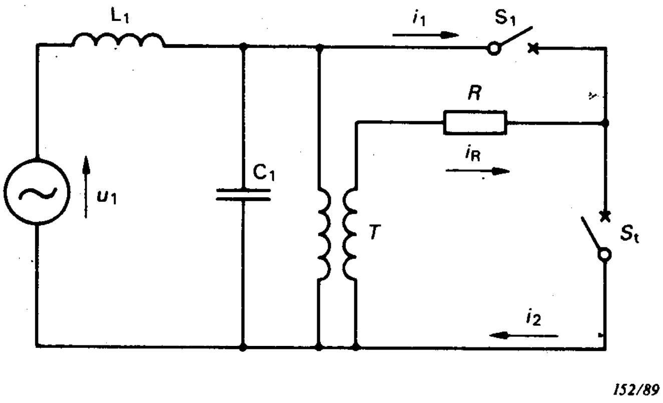


FIG. DD1. — Transformer or Skeats circuit.

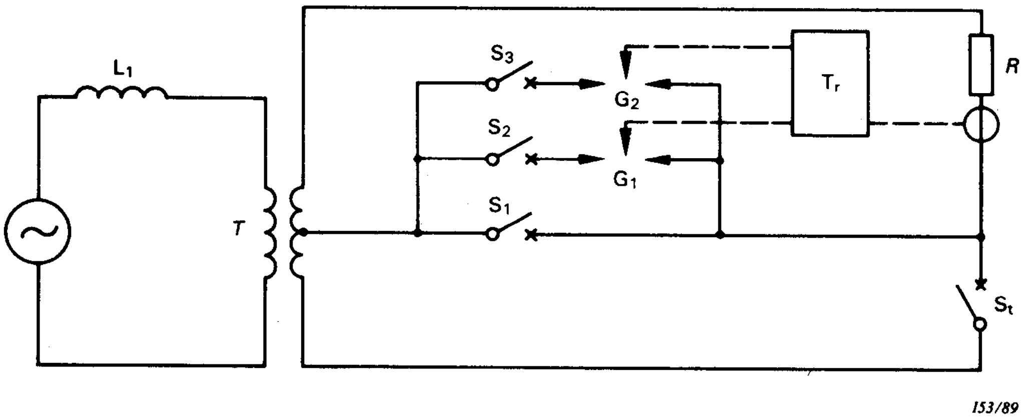


FIG. DD2. — Triggered transformer or Skeats circuit.

APPENDIX EE

INFORMATION TO BE GIVEN AND RESULTS TO BE RECORDED FOR SYNTHETIC TESTS

In addition to the requirements as specified in Appendix CC of IEC Publication 56, the following information shall be given in reports on synthetic tests:

EE1. Auxiliary circuit-breaker

a) Identification.

b) Description, including the number of units per pole, extinguishing medium and grading capacitors, if any.

EE2. Test conditions

a) Circuit parameters of the voltage circuit.

b) Setting of the intended arcing time of the test circuit-breaker including application of reignition circuit(s).

EE3. Quantities to be recorded

The resolution of the records with respect to the deflection and the time scale shall be such, that the information to be obtained can be evaluated with sufficient accuracy.

EE3.1 *Voltages*

a) Voltage of the current circuit.

b) Voltage across the test circuit-breaker.

c) Voltage across the auxiliary circuit-breaker.

d) Arc-voltage of the test circuit-breaker.

EE3.2 *Currents*

a) Current through the test circuit-breaker.

b) Current from the voltage circuit.

Notes 1. — For some quantities it may be necessary to have several records with different deflections and/or time scales. Normally it will be the case for the measurements EE3.1*b)* and EE3.2*a)*.

2. — Other information and records may be added to obtain test or design data.

APPENDIX FF

SPECIAL PROCEDURES FOR TESTING CIRCUIT-BREAKERS HAVING PARALLEL BREAKING RESISTORS

FF1. Introduction

When using synthetic test methods on circuit-breakers fitted with parallel breaking resistors, each arrangement should be considered on its merits, the guiding principle being that the synthetic test circuit should have a prospective transient recovery voltage as specified in IEC Publication 56 and a recovery voltage as specified in Sub-clause 4.1.3 of this standard should be applied to the circuit-breaker.

For those circuit-breakers where parallel resistors are employed to modify the shape of the transient recovery voltage, a synthetic test circuit should be such that the shape of the transient recovery voltage will be, as far as possible, the same as the specified transient recovery voltage as modified by the circuit-breaker resistor. If the ohmic value of the shunt resistor is very low, it may not be possible for the actual peak TRV in a synthetic test to attain this value due to the limited energy available from the voltage source. In this case, a modified test method should be chosen where this relative reduction of the actual peak TRV is kept to a negligible minimum (less than 5%). However, it may then still not be possible to meet the recovery voltage requirements of Sub-clause 4.1.3.

Valid tests may be made after observing certain precautions, e.g. by one of the following methods:

- by an adjustment of the parameters of the voltage circuit to provide the necessary additional energy absorbed by the resistor;
- by switching over to an additional a.c. voltage source capable of maintaining the voltage across the resistor;
- by disconnecting the test circuit-breaker shunt resistor, and connecting a resistor at other appropriate places in the test circuit (e.g. across the voltage circuit inductance) to give an equivalent transient recovery voltage waveform across the terminals of the test circuit-breaker. When using this method, care shall be taken to ensure that the influence of the resistor during the current-zero period is sufficiently close to that which would occur in a test with the resistor connected to the circuit-breaker terminals.

The choice and acceptance of such methods require very careful consideration and shall be subject to agreement between testing station, manufacturer and user.

If the applied test method does not subject the resistor to the full thermal stress, or the interrupter of the resistor current to its full breaking stress, then additional tests shall be made (see Sub-clauses FF3.3 and FF3.4).

FF2. Conditions

The requirements which relate to the basic synthetic test circuit, see Sub-clause 4.1, shall be met. Additional requirements during the high-voltage interval which must be met when the circuit-breaker resistance is so low as to preclude the use of a voltage source derived only from capacitors are given below.

FF2.1 *Transient recovery voltage interval*

The correct transient recovery voltage should appear across the circuit-breaker taking into account the influence of the shunt resistor incorporated in the circuit-breaker and the arc-voltage. There should be no discontinuity in the transient recovery voltage waveform.

Note. — The transient recovery voltage influenced only by the shunt resistor can be calculated by assuming an ideal circuit-breaker and evaluating the influence of the shunt resistor incorporated in the circuit-breaker on the specified transient recovery voltage.

FF2.2 *Power-frequency recovery voltage interval*

A power-frequency recovery voltage shall be provided which is the same as the value specified in IEC Publication 56.

Note. — It is acceptable to use a power-frequency recovery voltage of the correct amplitude which has a phase shift different from that which would be obtained in a network. The direction of this phase shift should be such that the recovery voltage in the synthetic test lags behind that of the network. The result is to extend the first loop of the recovery voltage, which is acceptable provided that the phase shift does not exceed about 20°.

FF3. **Multiple step test procedure**

An alternative approach is to use a set of four separate test procedures to establish that the overall testing of the test circuit-breaker is satisfactory. For this to be achieved it must be possible to disconnect the resistor(s) in the circuit-breaker.

Note. — It is essential that the operation and performance of the resistor interrupter is not affected by the operation of the main interrupter for these separate test procedures to be allowable.

FF3.1 *Thermal reignition mode tests on the main interrupter*

The object of these tests is to establish that reignitions do not occur in the main interrupter during the interaction interval.

A synthetic test is made with the resistor mounted in its normal position in the circuit-breaker. This test is subject to the normal requirements during an interval large with respect to the interaction interval.

When the current injection method with the voltage circuit in parallel with the test circuit-breaker is used, energy from the voltage source is usually sufficient if the discharge time constant of the voltage source with parallel breaking resistor of the circuit-breaker is at least five times higher than the duration of the interaction interval.

FF3.2 *Dielectric reignition mode tests on the main interrupter*

The resistor is first disconnected in the circuit-breaker. A synthetic test is then made with the correct prospective transient recovery voltage, as modified by the effect of the resistor only. This test covers the dielectric interval not already covered in the thermal reignition test described in FF3.1.

Notes 1. — One easement is allowed, namely that the substituting resistor in the external circuit can be switched into the circuit just prior to the beginning of the interaction interval if so desired. This may change the conditions determining the thermal reignition criteria but these have already been met in the test of Sub-clause FF3.1.

2. — Problems can arise when carrying out the dielectric test of Sub-clause FF3.2 on a number of series interrupters. The disconnection of the shunt resistors means that there is no longer any voltage grading apart from that provided by capacitance. This in itself may not provide a sufficiently uniform distribution and there is a danger of overstressing one interrupter. One way of overcoming this problem on open-type circuit-breakers is to attach an external string of higher value resistors to achieve near uniform grading. The effect of these shall of course be taken into account in providing the correct transient recovery voltage waveform.

FF3.3 *Tests on resistor*

Power frequency tests are required to demonstrate that the resistor can meet the thermal and voltage conditions imposed by the duty cycle of the circuit-breaker.

FF3.4 *Tests on resistor interrupter(s)*

Tests shall be made to demonstrate that the resistor interrupter(s) has (have) the required performance.

FF4. Additional remarks

It should be noted that with a circuit using power-frequency recovery voltage the timing of the make switch in the voltage circuit is critical and that correct operation of the testing procedure depends on this timing being maintained within close tolerances. Failure to observe this precaution can result in significant errors in the prospective transient recovery voltage waveform.

If the alternative multiple step procedure is adopted it should be noted that problems can arise during the dielectric reignition mode tests of Sub-clause FF3.2. The use of a substitute resistor external to the circuit-breaker can introduce parasitic inductance and capacitance into the circuit containing the main interrupter. This could lead to a thermal mode failure during the dielectric mode test. Such failures would not constitute a reason for rejection of the circuit-breaker but would require further dielectric mode tests following circuit modification.

The figures and equations given in this appendix are based on the paper: "Requirements for capacitive current switching tests employing synthetic test circuits for circuit-breakers without shunt resistors", published in *Electra* No. 87, March 1983. They are reproduced, with a few amendments, with the kind permission of the CIGRÉ.

APPENDIX GG

SYNTHETIC METHODS FOR CAPACITIVE-CURRENT SWITCHING

GG1. **Introduction**

Synthetic making and breaking capacitive current tests are generally made single phase.

As the stress of the breaker during capacitive current making operations is small—with the exception of back-to-back capacitor bank switching—they may be performed separately.

The phenomena of reigniting and restriking cause interactions between the source and the capacitive load which are, at present, difficult to simulate reliably by synthetic testing circuits. Therefore, the synthetic method may only validate a restrike-free operation. After a reignition or restrike the circuit conditions would not be meaningful and direct testing would be required.

The phenomenon of pre-striking allows for the possibility of interruption of high frequency current during the closing operation. Such an interruption will be followed by reignition and would indicate that the circuit-breaker may require direct testing.

When switching long unloaded lines, travelling wave phenomena may arise, the simulation of which by synthetic circuits is possible using the envelope. However, a closer simulation is possible by introducing additional circuits which are under consideration. Circuit-breakers equipped with opening resistors may be tested in two part synthetic test circuits, where the circuit parameters are adjusted to give recovery voltages equivalent to the stress of a direct test circuit.

GG2. **Requirements concerning synthetic break-tests**

In order to take into account the phenomena relating to interrupting capacitive currents, the following items shall comply with the existing specifications:

1) the shape and amplitude of the power-frequency test current, particularly in the final loop before interruption;
2) the shape and amplitude of the power-frequency supply voltage;
3) the voltage on the load side after interruption;
4) the magnitude, frequency and damping of the transient voltage during the voltage jump, when testing under conditions simulating a high source impedance;
5) the electrical field configuration across the gap and to earth.

GG3. **Requirements concerning synthetic make-tests**

In order to take into account the phenomena relating to making capacitive currents, the following items shall comply with the existing specifications:

1) the amplitude and the shape of the applied voltage on the source side;
2) the value of the trapped charge on the load side (under usual conditions this value is zero). When closing against a trapped charge the initial conditions of the load side have to be taken into account, and a proper modification of the synthetic make circuit may be necessary;

GG4. Current chopping

Current chopping phenomena, caused by interaction between the circuit-breaker and the test circuit, generally lead to a reduction of the load-side voltage and thus also of the dielectric stress of the test object.

In direct test circuits, chopping of small capacitive test currents may take place. In synthetic testing circuits the probability for these events is increased for the following reasons:

- generally speaking the characteristic parameters of the main and stray components of the test circuits are different. Therefore the chopping behaviour of the circuit-breaker may be changed;
- the effect of additional (auxiliary) circuit-breakers in series with the test circuit-breaker;

- the increased ratio of arc-voltage to power-frequency voltage.

Therefore, when performing synthetic tests it may be difficult to determine whether or not current chopping is a significant feature of the test circuit-breaker. To reduce current chopping, the following means are applicable:

- modify the capacitances seen from the circuit-breaker terminals;
- use a special auxiliary circuit-breaker with short minimum arc-duration and low arc-voltage.

GG5. Synthetic test circuits

GG5.1 *Basic circuits for breaking tests*

Synthetic testing circuits principally consist of two combined circuits, a current circuit and a voltage circuit. For capacitive current switching, both circuits may have a capacitive nature, although an inductive or ohmic current circuit in some cases can be used as an alternative provided that the phase angle between the two sources is changed accordingly.

These two sources can be generator fed transformers or charged capacitors, or a combination of both. The application of synthetic circuits implies the use of an auxiliary breaker to isolate the test circuit-breaker from the current circuit.

The connection of the two sources to the two breakers can be in a parallel mode, subtracting the voltages on the auxiliary breaker, or in series mode, adding the voltages on the test circuit-breaker.

Depending on whether the voltage circuit is connected permanently or switched in at a moment before or after power-frequency current-zero, a distinction can be made between power-frequency current superposition, current injection or voltage injection circuits. For tests under conditions of high source impedance a transient "jump" voltage can be generated by the current or the voltage circuit, preferably at the terminal of the breaker where the a.c. voltage is applied. The other terminal of the breaker has to be stressed by a slowly decaying d.c. voltage.

In some test circuits both voltages are superimposed at one terminal of the breaker, the other terminal being earthed. This condition is more severe for the insulation to earth. For metal-enclosed circuit-breakers an additional voltage source may be connected to the tank to compensate for this effect.

Many test circuits are possible with different features. Some examples are given in Figures GG1 to GG5. (See *Electra* No. 87 - March 1983.)

GG5.2 *Basic synthetic test circuits for the making test*

For a synthetic capacitive making test, the voltage circuit supplies the test voltage during the closing of the contacts till the moment of dielectric breakdown, and subsequently the initial transient making current. For this purpose some special elements may be necessary.

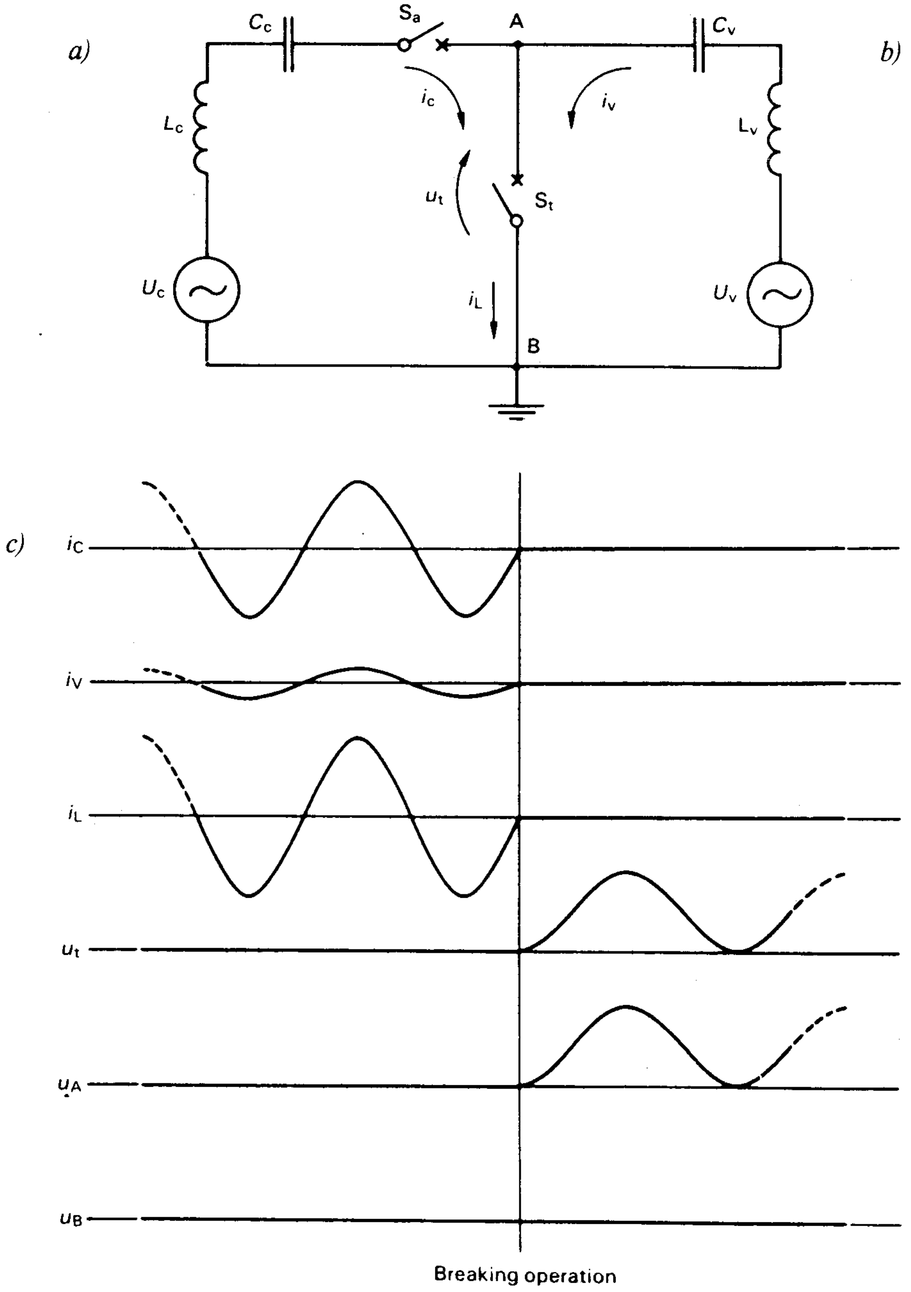
Immediately after the dielectric-breakdown, the current circuit has to be inserted to supply the transient making current, followed by the power-frequency current. For this purpose a gap is triggered early enough to sustain the pre-arcing current.

To deliver both the required transient making current and the power-frequency current, a capacitive current source is suitable, while an inductive current source is not, because it does not give the correct current shape. An example is given in Figure GG6. (See *Electra* No. 87 - March 1983.)

Note. — The formulae given with Figures GG1 to GG6 are not exact and are merely meant to give the approximate behaviour of the circuits.

APPLICABLE FOR FIGURES GG-1 TO GG-6:

a) general layout of the circuit
b) mathematical relations between circuit parameters
c) qualitative current and voltage shapes
n = the ratio between the specified test voltage U_s and the actual voltage of the current circuit U_c
m = the ratio between the specified test current I_L and the current supplied by the voltage circuit
u_t = voltage across test circuit-breaker S_t
u_A, u_B = voltage to earth at point A, B... respectively
U_h = charging voltage of voltage circuit
C_L = load capacitance



b)

Current circuit

Voltage $U_c = U_s/n$
Current $I_c = I_L(1 - 1/m)$
Inductance $\omega L_c \ll 1/\omega C_c$
Capacitance $C_c = n(1 - 1/m)\, C_L$
I_L = load current

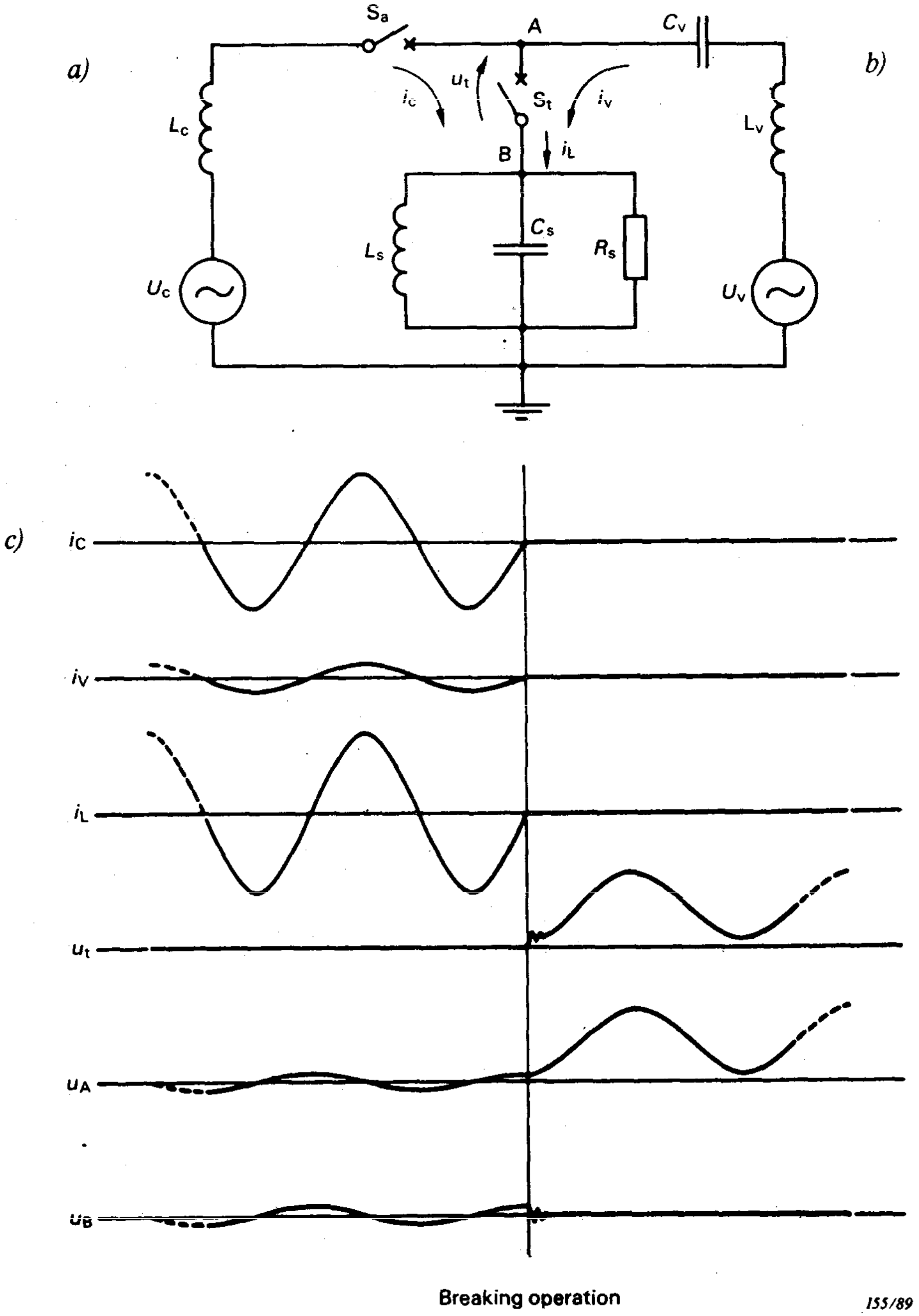
Voltage circuit

Voltage $U_v = U_s$
Current $I_v = I_L/m$
Inductance $\omega L_v \ll 1/\omega C_v$
Capacitance $C_v = C_L/m$
C_l = load capacitance

FIG. GG1. — Synthetic testing scheme (parallel mode).

The current circuit has a voltage U_c and a capacitance C_c to supply the capacitive current I_c.
The voltage circuit delivers the specified test voltage U_v and a reduced capacitive current I_v by means of the capacitor C_v.

154/89



b)

Current circuit

Voltage $U_c = -U_s/n$
Current $I_c = I_L(1 - 1/m)$

Inductance $\omega(L_c + L_s) = \dfrac{1}{n(1 - 1/m)\,\omega C_L}$

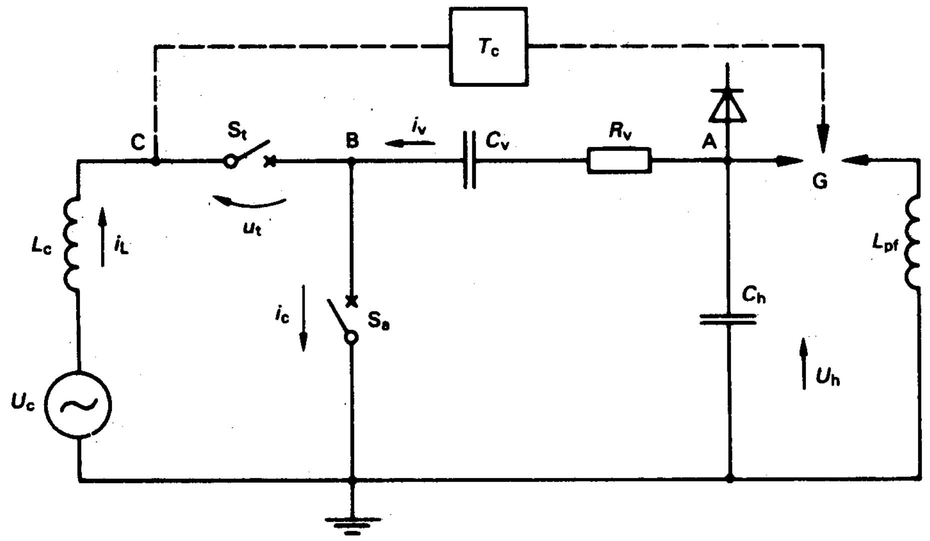
Voltage circuit

Voltage $U_v = U_s$
Current $I_v = I_L/m$
Capacitance $C_v = C_L/m$
Inductance $\omega L_v \ll 1/\omega C_v$

FIG. GG2.— Synthetic testing scheme with an inductive current circuit and with facility to adjust a voltage jump.

In order to obtain a voltage jump the elements R_s, L_s and C_s have to be inserted between the test circuit-breaker and earth.

a)



b)

	Current circuit	Voltage circuit
Voltage	$U_c = U_s/n$	$U_h = U_s \cdot \sqrt{2}$
Current	$I_c = I_L$	$i_v = 0$
Inductance	$\omega L_c = 1/n\omega C_h$	$L_{pf} = 1/\omega^2 \cdot C_h$

c)

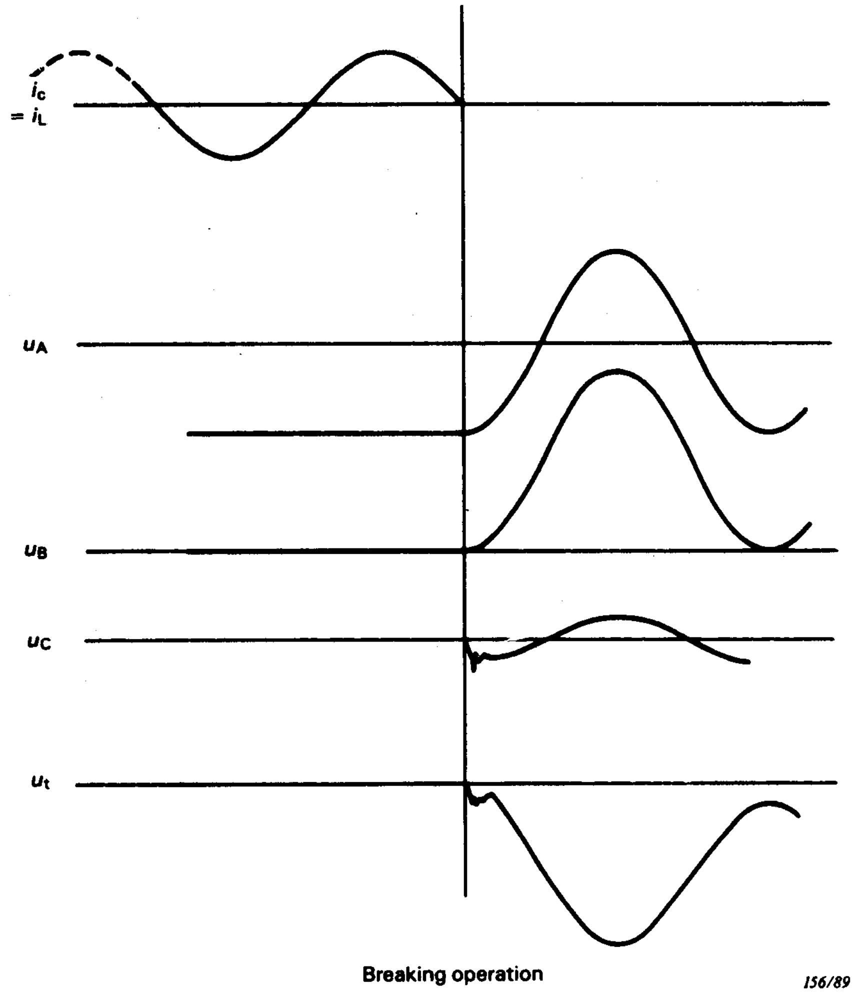
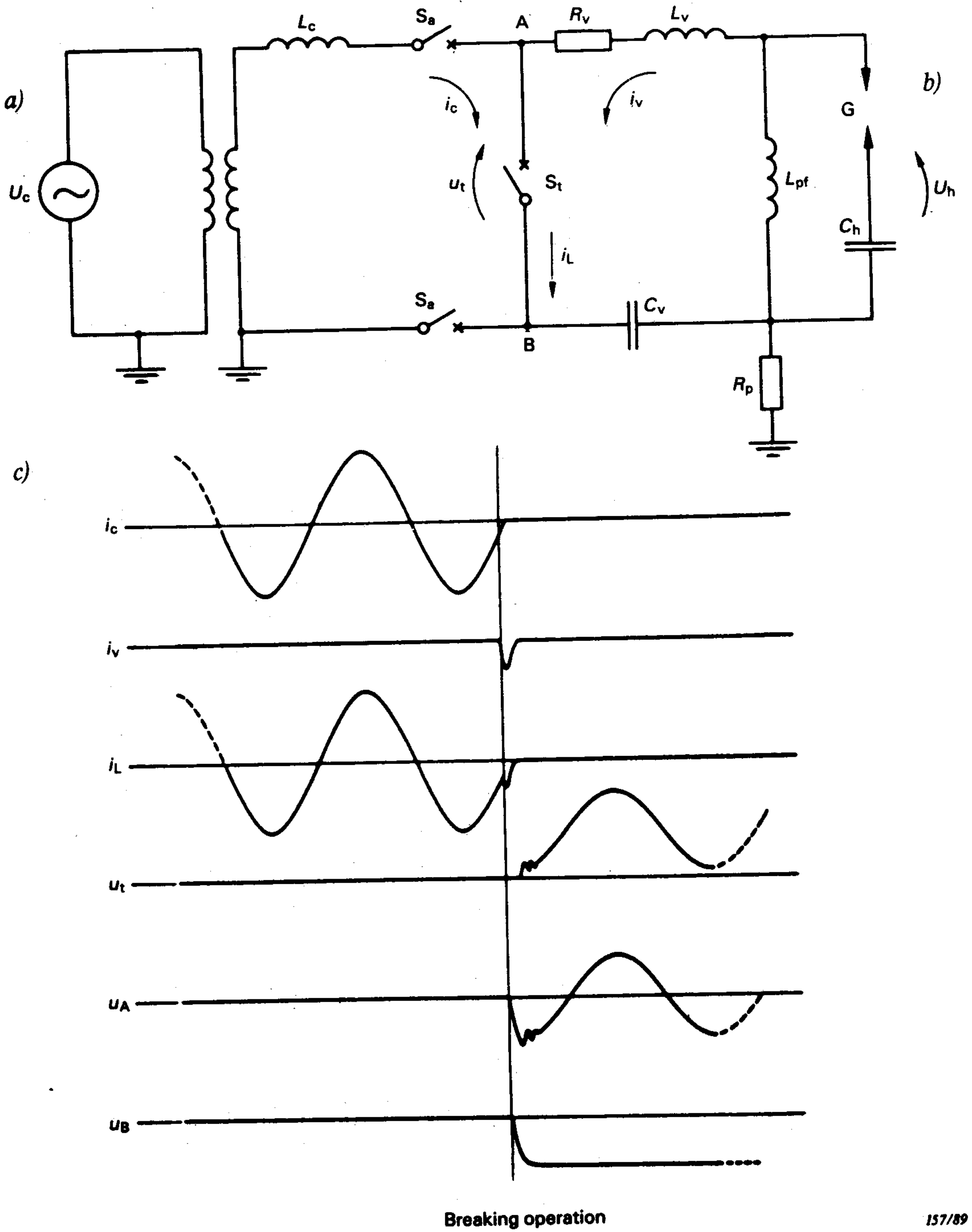


FIG. GG3.— Synthetic voltage injection circuit providing a voltage jump.



b)

Current circuit

Voltage $U_c = U_s/n$

Current $I_c = I_L$

Inductance $\omega L_c = 1/n\omega C_L$

Voltage circuit

Voltage $U_h = \frac{C_v + C_h}{C_h} U_s \cdot \sqrt{2}$

Current $i_v = \frac{U_h}{\omega_o L_v} \cdot e^{-at} \cdot \sin \omega_o t$

where:

$a = \frac{R_v}{2L_v}$

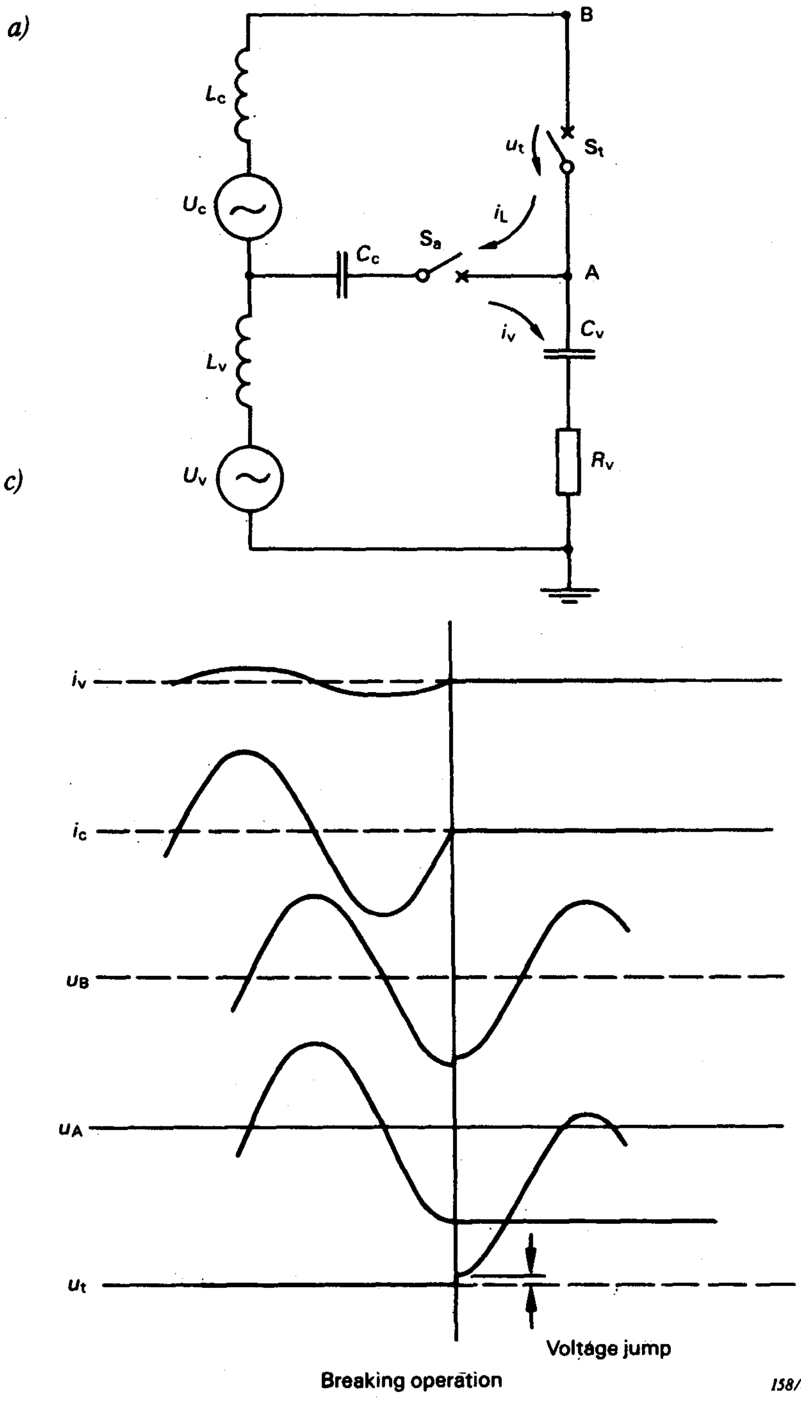
$\omega_o = \frac{1}{L_v}\left(\frac{1}{C_h} + \frac{1}{C_v}\right) - \left(\frac{R_v}{2L_v}\right)^2$

$\hat{t}$ = Time to peak of the injected current

Inductance $L_v = \frac{U_h}{I_L \cdot \omega \cdot \sqrt{2}}$

Voltage jump $= U_h \cdot e^{-\frac{\pi a}{\omega_o}}$

FIG. GG4. — Synthetic current injection scheme.



b)

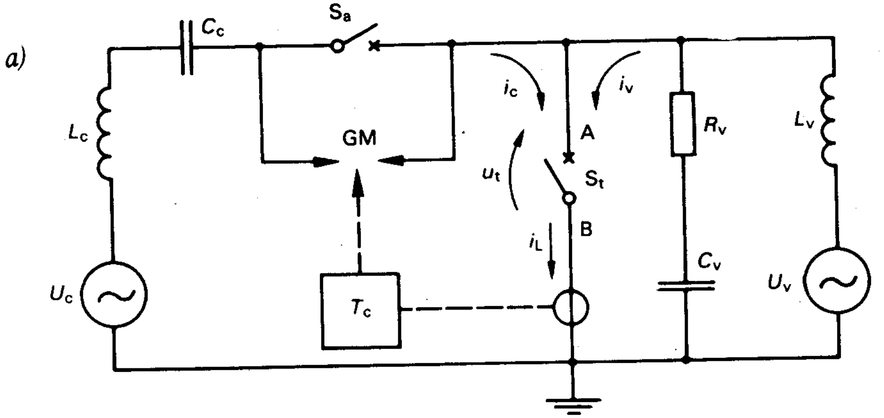
Current circuit

Voltage $U_c = U_s/n$
Current $I_c = U_c\omega C_c$
Inductance $\omega L_c \ll 1/\omega C_c$
Capacitance $C_c = nC_L$
i_L = load current

Voltage circuit

Voltage $U_s = U_c + U_v$
Current $I_v = U_s\omega C_v$
Inductance $\omega L_v \ll 1/\omega C_v$
Capacitance $C_v = C_L/m$

FIG. GG5. — Synthetic test circuit (serial mode) to apply to both sides of the test breaker the normal system recovery voltage.



b)

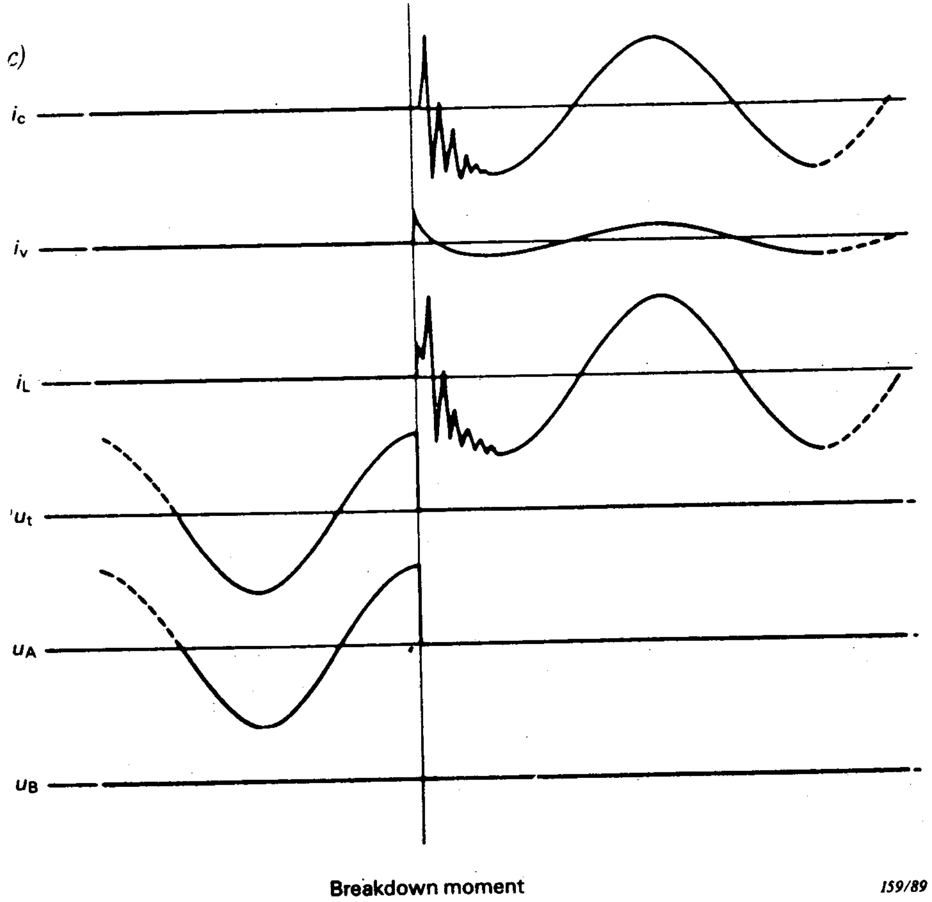
Current circuit

Voltage $U_c = U_s/n$
Current $I_c = I_L$
Inductance $L_c = L_s/n$
Capacitance $C_c = nC_L$

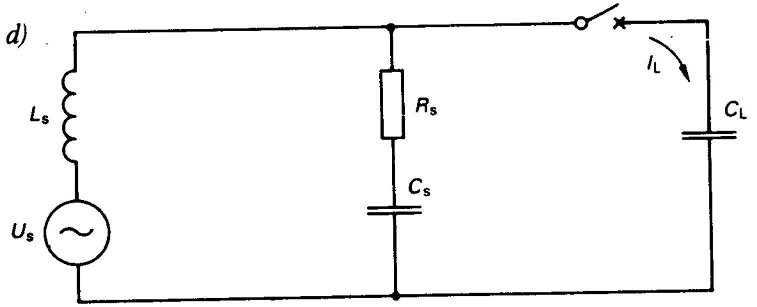
Voltage circuit

Voltage $U_v = U_s$
Current $I_v = U_v/\omega L_v$
Capacitance $C_v = C_s$
Resistance $R_v = R_s$

R_s and C_s define the initial transient making current
L_s and C_L define the transient making current



159/89



Equivalent circuit diagram for defining R_s, C_s and L_s

FIG. GG6.— Synthetic testing scheme for making.

APPENDIX HH

SYNTHETIC METHODS FOR THREE-PHASE TESTING

HH1. General

When all three poles of a circuit-breaker are in the same enclosure, some interactions may occur between phases due to distribution of transient electric stresses or electrodynamical forces on arcs of adjacent phases, and even to physical interactions of extinguishing media (i.e. hot gases).

In such cases, three-phase testing has obviously to be performed.

In testing plants it may be difficult to obtain the required three-phase short-circuit power and circuits for the higher rated voltages.

Various testing circuits are proposed for testing high-voltage three-phase circuit-breakers. Most of them do not correctly stress the circuit-breaker. Circuits must therefore be agreed upon between user and manufacturer. Nevertheless, some conditions are listed below.

HH2. Validity conditions

The test has to take into account the stresses in the interrupting elements, the ones between poles and the ones between poles and the enclosure, taking advantage of two or multiple part testing procedure.

The following conditions shall be met:

1) Full three-phase current shall be supplied to the three-pole circuit-breaker under test.
2) A synthetic circuit capable of producing equivalent stresses with respect to all the periods of the interrupting process shall be applied to the first pole to clear.
3) The TRV for the last clearing poles shall be in correct phase relation; the requirements during the interaction interval for the last poles to clear may be relaxed.

   It is emphasised that no requirements are given in IEC Publication 56 concerning the TRV waveshapes for the last poles to clear. It is proposed, provisionally, in case of necessity, to consider the same waveshape as for the first pole to clear but the amplitude being multiplied by $\sqrt{3}/2h$, where h is the first pole factor.

4) The recovery voltage should preferably be a.c. with proper duration, and applied across at least two adjacent poles.
5) If necessary, a multiple part testing procedure is allowed. The test may be repeated with some changed conditions to simulate the different stresses. Agreement between user and manufacturer is necessary and the procedure shall be fully described in the test report.
6) The enclosure shall be earthed at one point only.
7) Other general requirements of IEC Publication 56 or those concerning synthetic testing apply, especially the arc-duration conditions (with possible forced reignition), and the consideration of the influence of mechanical forces in the three poles due to operating mechanism.

APPENDIX JJ

REIGNITION METHODS TO PROLONG ARCING

JJ1. Method with multiple application of the voltage source

With this method, the voltage source is connected to the test circuit-breaker at each current-zero. If the test circuit-breaker clears at a zero, the procedure is stopped. If the test circuit-breaker reignites, then the current source is reconnected by reigniting the auxiliary breaker. At the same time, the voltage source will be disconnected and then reconnected at the next current-zero, with its polarity reversed appropriately.

If the single voltage source has insufficient energy for successive application at several current-zeros, it will be necessary to have several voltage sources: one for each reignition plus one to apply the TRV at the final current-zero.

This method involves practically the same procedure as for direct testing, taking into account the relationship between breaking at the first zero and breaking at a following zero.

JJ2. "Step-by-step" method

With this method, only one voltage source is used. The test circuit-breaker is reignited by a special reignition circuit, or other means, in order to prolong arcing up to the current-zero at which the voltage source is to be applied. This "step-by-step" method needs less additional installations compared to the above mentioned method. However, more tests may be necessary to comply with the specified arcing times. The method is considered to be a sufficiently close approximation of the direct testing procedure. As this method makes it possible to force reignition of the test circuit-breaker in all conditions, special care shall be taken not to reignite the circuit-breaker at the instant of a current-zero when the circuit-breaker can clear. For this purpose it is necessary to determine beforehand, the minimum arcing-time of the circuit-breaker. Two breaking tests with arcing times, just below and just above (i.e. ± 1 ms) the minimum arcing time are satisfactory for this determination.

1) Method with higher power-frequency circuit severity

In some cases, the arcing of the test circuit-breaker may be prolonged by delaying the opening of the auxiliary circuit-breaker or by increasing the rate-of-rise of the transient recovery voltage in the power-frequency current circuit. Whether this is effective or not depends upon the characteristics of the power-frequency current circuit and of the circuit-breaker under test.

2) Method with a separate reignition-circuit

A separate reignition-circuit provides a rapidly rising pulse of current of opposite polarity to that of the power-frequency current, approximately 10 μs before current-zero. The current through the circuit-breaker is thus rapidly reversed and conduction in the arc-gap is maintained for a further loop of power-frequency current. As an example, a multi-loop reignition circuit is indicated in Figure JJ1. Several such circuits may be used for prolonging the arcing through several loops of current. The reignition circuit can be applied to reignite both test and auxiliary circuit-breaker. However, the need to reignite both circuit-breakers can sometimes be avoided by suitably delaying the separation of the auxiliary circuit-breaker contacts.

JJ3. Method using duplicate (Skeats) circuit

A circuit arrangement is shown in Figure JJ2 and the corresponding current and voltage for an asymmetrical test in Figure JJ3.

At the first current-zero the test circuit-breaker is stressed by the Skeats circuit thus achieving a late dielectric reignition; in such a way the short-circuit current waveform is equivalent to that of a direct test. At the second current-zero the current injection circuit is applied to the test circuit-breaker.

First current zero:

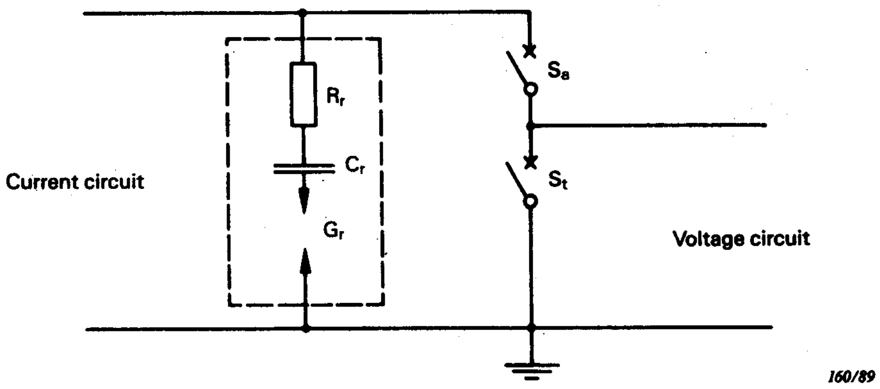
S_1 is opened and acts as auxiliary breaker
G2 is triggered when a reignition occurs
S_2 remains closed
S_3 remains closed
S_4 remains open

During the high current interval:

S_3 is opened
S_4 is closed

Second current-zero:

S_1 remains open
S_2 is opened and acts as auxiliary breaker
G1 is triggered.



S_t = test circuit-breaker

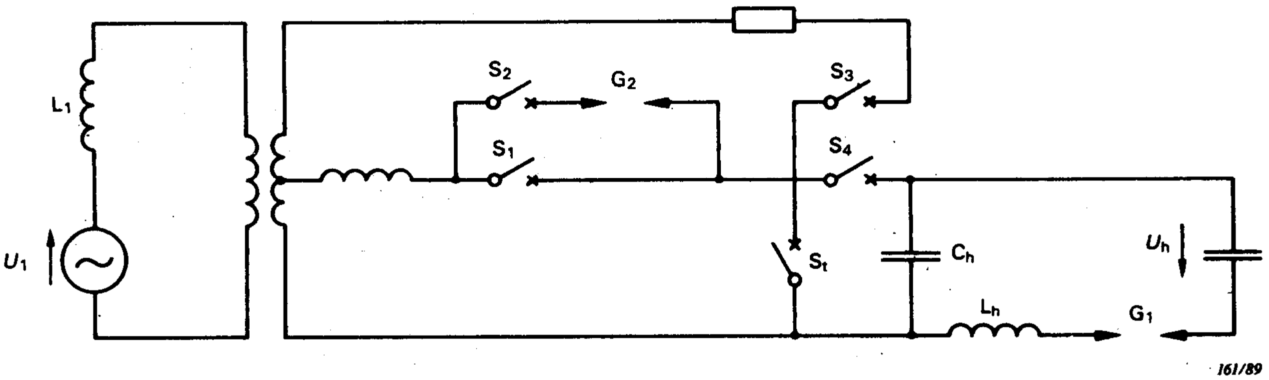
S_a = auxiliary circuit-breaker

R_r = resistor for reignition circuit

C_r = capacitor for reignition circuit

G_r = spark gap for closing reignition circuit

FIG. JJ1.— Typical reignition circuit diagram for prolonging arc-duration.



U_1 = voltage of current circuit

L_1 = inductance of current circuit

S_1 S_2 S_3 S_4 = auxiliary circuit-breakers

S_t = test circuit-breaker

L_h = inductance of voltage circuit

C_h = capacitance of voltage circuit which together with L_h controls the major part of the TRV

U_h = charging voltage of voltage circuit

G_1 G_2 = spark gaps

FIG. JJ2.— Combined Skeats and current injection circuits.

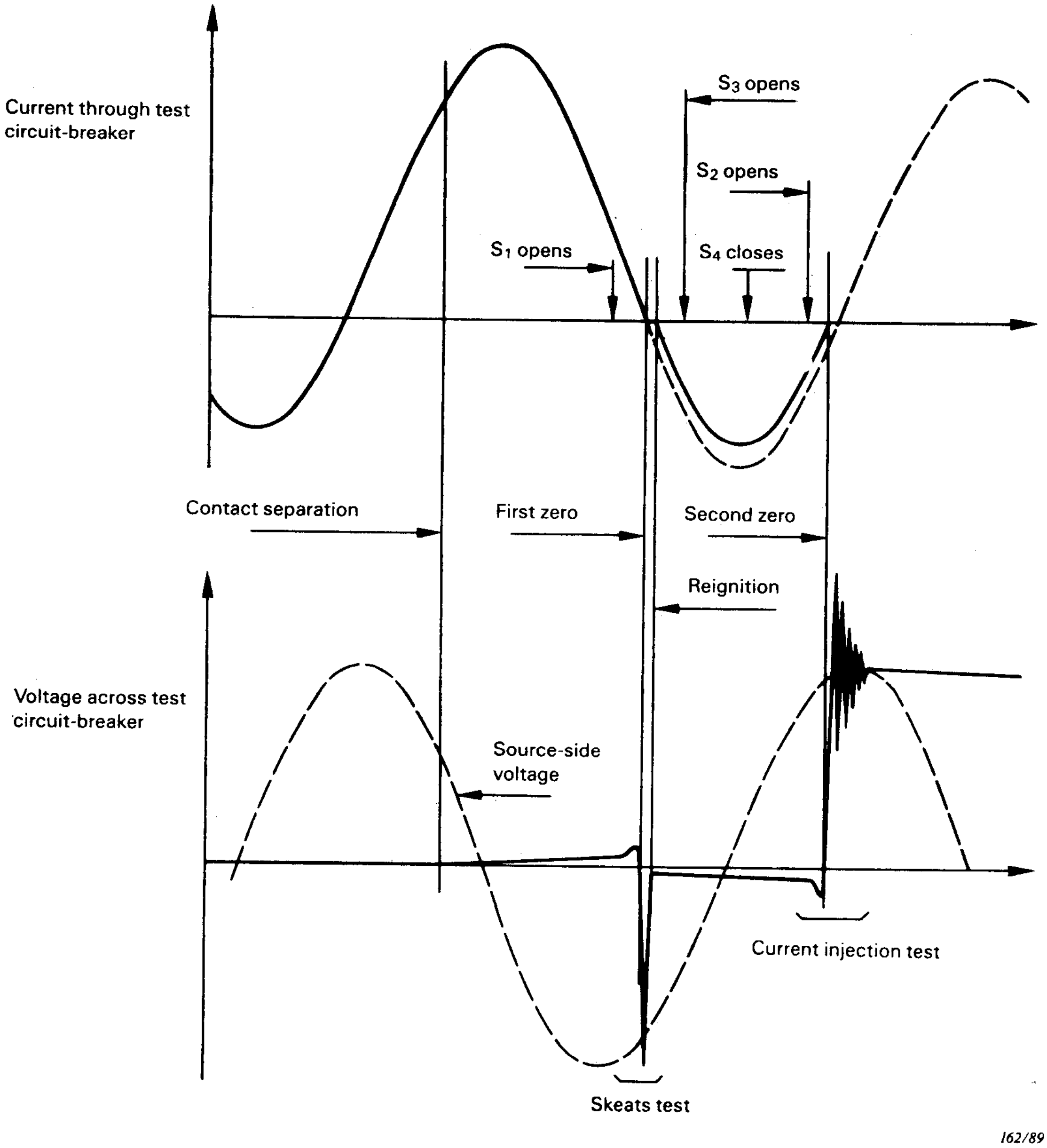


FIG. JJ3.— Typical waveforms obtained on an asymmetrical test using the circuit in Figure JJ2.

Printed at Dee Kay Printers, New Delhi, India

(Continued from second cover)

Page

APPENDIX BB Current injection methods 40

APPENDIX CC Voltage injection methods 45

APPENDIX DD Duplicate circuit (transformer or Skeats circuit) ... 48

APPENDIX EE Information to be given and results to be recorded for synthetic tests 51

APPENDIX FF Special procedures for testing circuit-breakers having parallel breaking resistors 52

APPENDIX GG Synthetic methods for capacitive-current switching ... 55

APPENDIX HH Synthetic methods for three-phase testing ... 64

APPENDIX JJ Reignition methods to prolong arcing 65

NATIONAL FOREWORD

This Indian Standard which is identical with IEC Pub 427 (1989) 'Synthetic testing of high-voltage alternating current circuit-breakers' issued by the International Electrotechnical Commission (IEC), was adopted by the Bureau of Indian Standards on the recommendation of the High Voltage Switchgear and Controlgear Sectional Committee (ET 08) and approval of the Electrotechnical Division Council.

This standard is intended to serve as a guide for synthetic testing methods of HV ac circuit-breakers in accordance with requirements for making and breaking capacities over the range of test duties described in IS 13118 : 1991, which is identical to IEC Pub 56. There is at present inadequate experience in the application of synthetic testing methods. The committee responsible for this standard had felt that publication of this Indian Standard in line with the IEC work would facilitate acquisition of experience. It has considered the text of this standard in depth and approved the same as suitable for publication as Indian Standard.

CROSS REFERENCES

In this Indian Standard, the following international standard is referred. In its place, read the following:

International Standard	*Corresponding Indian Standard*	*Degree of Equivalence*
IEC Pub 56 (1987) High voltage alternating-current circuit-breakers	IS 13118 : 1991 High voltage alternating current circuit-breakers	Identical

Standard Mark

The use of the Standard Mark is governed by the provisions of the ***Bureau of Indian Standards Act, 1986*** and the Rules and Regulations made thereunder. The Standard Mark on products covered by an Indian Standard conveys the assurance that they have been produced to comply with the requirements of that standard under a well defined system of inspection, testing and quality control which is devised and supervised by BIS and operated by the producer. Standard marked products are also continuously checked by BIS for conformity to that standard as a further safeguard. Details of conditions under which a licence for the use of the Standard Mark may be granted to manufacturers or producers may be obtained from the Bureau of Indian Standards.

Bureau of Indian Standards

BIS is a statutory institution established under the *Bureau of Indian Standards Act, 1986* to promote harmonious development of the activities of standardization, marking and quality certification of goods and attending to connected matters in the country.

Copyright

BIS has the copyright of all its publications. No part of these publications may be reproduced in any form without the prior permission in writing of BIS. This does not preclude the free use, in the course of implementing the standard, of necessary details, such as symbols and sizes, type or grade designations. Enquiries relating to copyright be addressed to the Director (Publications), BIS.

Revision of Indian Standards

Indian Standards are reviewed periodically and revised, when necessary and amendments, if any, are issued from time to time. Users of Indian Standards should ascertain that they are in possession of the latest amendments or edition. Comments on this Indian Standard may be sent to BIS giving the following reference:

Doc : No ET 08 (3623)

Amendments Issued Since Publication

Amend No.	Date of Issue	Text Affected

BUREAU OF INDIAN STANDARDS

Headquarters:

Manak Bhavan, 9 Bahadur Shah Zafar Marg, New Delhi 110002
Telephones : 331 01 31, 331 13 75
Telegrams : Manaksanstha
(Common to all Offices)

Regional Offices :	Telephone
Central : Manak Bhavan, 9 Bahadur Shah Zafar Marg NEW DELHI 110002	331 01 31 331 13 75
Eastern : 1/14 C. I. T. Scheme VII M, V. I. P. Road, Maniktola CALCUTTA 700054	37 84 99, 37 85 61 37 86 26, 37 86 62
Northern : SCO 445-446, Sector 35-C, CHANDIGARH 160036	53 38 43, 53 16 40 53 23 84
Southern : C. I. T. Campus, IV Cross Road, MADRAS 600113	235 02 16, 235 04 42, 235 15 19, 235 23 15
Western : Manakalaya, E9 MIDC, Marol, Andheri (East) BOMBAY 400093	632 92 95, 632 78 58, 632 78 91, 632 78 92

Branches : AHMADABAD, BANGALORE, BHOPAL, BHUBANESHWAR, COIMBATORE FARIDABAD, GHAZIABAD, GUWAHATI, HYDERABAD, JAIPUR, KANPUR LUCKNOW, PATNA, THIRUVANANTHAPURAM.

Printed at Dee Kay Printers, New Delhi, India